1. Introduction

1.1 Scope

This version of the ICD is the version generated after qualification campaign closure.

This specification details the ratings, physical, geometrical, electrical and electro-optical characteristics, test- and inspection-data for the High Accuracy Star Tracker (HAS) Version 2 CMOS Active Pixel image Sensor (CMOS APS).

The device described in this document is protected by US patent 6,225,670 and others.

1.2 Component Type Variants

A summary of the type variants of the basic CMOS image sensor is given in Table 1 on page 8. The complete list of detailed specifications for each type variant is given in Table 3 on page 9 for each type separately.

All specifications in Table 3 on page 9 are given at 25 ± 3°C, under nominal clocking and bias conditions. Exceptions are noted in the 'remarks' field.

1.3 Maximum Rating

The maximum ratings which shall not be exceeded at any time during use or storage are as scheduled in Table 2 on page 9.

1.4 Physical Dimensions and Geometrical Information

The physical dimensions of the assembled component are shown in Figure 2 on page 25. The geometrical information in Figure 4 on page 26 describes the position of the die in the package.

1.5 Pin Assignment

Figure 6 on page 27 contains the pin assignment. The figure contains a schematic drawing and a pin list. A detailed functional description of each pin can be found in "Pin List" on page 39.

1.6 Soldering Instructions

Soldering is restricted to manual soldering only. No wave or reflow soldering is allowed. For the manual soldering, following restrictions are applicable:

- Solder 1 pin on each of the 4 sides of the sensor.
- Cool down period of min. 1 minute before soldering another pin on each of the 4 sides.
- Repeat soldering of 1 pin on each side, including a 1 minute cool down period.

1.7 Handling Precautions

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling. The following guidelines are applicable:

- Always manipulate the devices in an ESD controlled environment.
- Always store the devices in a shielded environment that protects against ESD damage (at least a non-ESD generating tray and a metal bag).
- Always wear a wrist strap when handling the devices and use ESD safe gloves.
- The HAS2 is classified as class 1A (JEDEC classification - [AD03]) device for ESD sensitivity.

1.8 Storage Information

The components must be stored in a dust-free and temperature-, humidity and ESD controlled environment.

- Devices must always be stored in special ESD-safe trays such that the glass window is never touched.
- The trays are closed with EDS-safe rubber bands.
- The trays are sealed in an ESD-safe conductive foil in clean room conditions.
- For transport and storage outside a clean room the trays are packed in a second ESD-save bag that is sealed in clean room.

1.9 Procurement Requirements

The HAS2 image sensor can be procured at Cypress Semiconductor or its distributors, using the following references:

- Flight sensors: CYIH1SM1000AA-HHCS.
- Engineering sensors: CYIH1SM1000AA-HHCES.

The HAS sensor is subject to the standard European export regulations for dual use products.

A Certificate of Conformance will be issued upon request at no additional charge. The CoC will refer to this Detailed Specification.

Additional screening tests can be done upon request at additional cost.

The following data is by default delivered with FM sensors:

- Sensor calibration data
- Temperature calibration data
- Certificate of Conformance to this detailed specification
- Visual inspection report
- Bad pixel map

2. Ordering Information

Marketing Part Number	Description	Package	Production
CYIH1SM1000AA-HHCS	Space qualified (mono version)	84 pin JLCC	In production
CYIH1SM1000AA-HHCES	Standard Market (mono version)	84 pin JLCC	Nov-09

3. Applicable Documents

The following documents form part of this specification and shall be read in conjunction with it:

Nr.	Reference	Title	Issue	Date
AD01	ESCC Generic Specification 9020	Charge Coupled Devices, Silicon, Photosensitive	2 Draft F	
AD02	Cypress 001-06225[1]	Electro-optical test methods for CMOS image sensors	E	October, 2008
AD03	JESD22-A114-B	Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)	B	June, 2000
AD04	APS2-FVD-06-003	Process Identification Document for HAS2	2	February, 2008
AD05	Cypress 001-49283	Visual Inspection for FM devices	1	January, 2008
AD06	Cypress 001-49280	HAS2 FM Screening	2	June, 2009

4. Acronyms Used

For the purpose of this specification, the terms, definitions, abbreviations, symbols, and units specified in ESCC basic Specification 21300 shall apply. In addition, the following table contains terms that are specific to CMOS image sensors and are not listed in ESCC21300

Abbreviation	Description
ADC	Analog to Digital Convertor
APS	Active Pixel Sensor
CDS	Correlated Double Sampling
DNL	Differential Non Linearity
DR	Destructive Readout
DSNU	Dark Signal Non Uniformity
EPPL	European Preferred Parts List
ESD	Electro-Static Discharge
FPN	Fixed Pattern Noise
HAS	High Accuracy Startracker
INL	Integral Non Linearity
MTF	Modulated Transfer Function
NDR	Non Destructive Readout
PRNU	Pixel Response Non Uniformity
TBC	To be Confirmed
TBD	To be Defined
RGA	Residual Gas Analysis

Note
1. This specification will be superseded by the ESCC basic specification 25000 which is currently under development. The current reference is an internal Cypress procedure which is a confidential document.

The following formulas are applicable to convert % Vsat and mV/s into e- and e-/s:

$$FPN[e-] = \frac{FPN[\%Vsat] * \overline{Vsat}}{conversion\_gain}$$

$$Dark\_signal[e-/s] = \frac{Dark\_signal[V/s]}{conversion\_gain}$$

$$DSNU[e-] = \frac{DSNU[\%Vsat] * \overline{Vsat}}{conversion\_gain}$$

Other definitions:

$$ADC\ Quantization\ Noise = \frac{\frac{Ana\log Range}{ADC\,\mathrm{Re}\,solution}}{\frac{Conversion\,Gain}{\sqrt{ADC\,\mathrm{Re}\,solution}}}$$

- Conversion gain for HAS: 14.8 µV/e-
- Definition for Local measurements: 32 x 32 pixels
- Definition for Global measurements: Full pixel array

5. Detailed Information

5.1 Deviations from Generic Specification

Lot acceptance and screening are based on ESCC 9020 issue 2 draft F. section 5.9 on page 5 of this specification describes the lot acceptance and screening.

5.2 Mechanical Requirements

5.2.1 Dimension Check

The dimensions of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2 on page 25.

5.2.2 Geometrical Characteristics

The geometrical characteristics of the components specified herein shall be checked. They shall comply with the specifications and the tolerances as indicated in Figure 2 on page 25 and Figure 3 on page 26.

5.2.3 Weight

The maximum weight of the components specified herein shall be as specified in Table 3 on page 9 - Mechanical Specifications, item 2.

5.3 Materials and Finishes

The materials and finishes shall be as specified herein. Where a definite material is not specified, a material which will enable the components specified herein to meet the performance requirements of this specification shall be used.

5.3.1 Case

The case shall be hermetically sealed and have a ceramic body and a glass window.

Type	JLCC-84
Material	Black Alumina BA-914
Thermal expansion coefficient	7.6 x 10^{-6} /K
Hermeticity	< 5·10-7 atms. cm3/s
Thermal resistance (Junction to case)	3.633 °C/W

5.3.2 Lead material and finish

Lead material	KOVAR
1e Finish	Nickel, min 2 µm
2nd Finish	Gold, min 1.5 µm

5.3.3 Window

The window material is a BK7G18 glass lid with anti-reflective coating applied on both sides.

The optical quality of the glass shall have the following specification:

See Table 3 on page 9 - glass window specification

The anti reflective coating shall have a reflection coefficient < 1.3% absolute and < 0.8% on average, over a bandwidth from 440 nm to 1100 nm.

5.4 Marking

5.4.1 General

The marking Shall consist of a lead identification and traceability information.

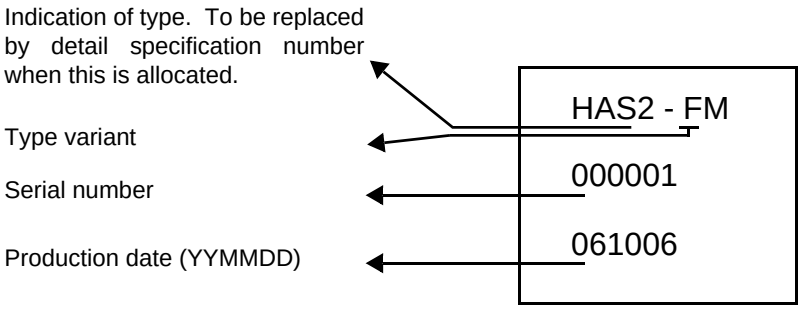
5.4.2 Lead Identification

An index to pin 1 shall be located on the top of the package in the position defined in Figure 2 on page 25. The pin numbering is counter clock-wise, when looking at the top-side of the component.

5.4.3 Traceability Information

Each component shall be marked such that complete traceability can be maintained.

The component shall bear a number that is constituted as follows:



5.5 Electrical and Electro-optical Measurements

5.5.1 Electrical and Electro-optical Measurements at Reference Temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table 4 on page 14 and Table 13 on page 24. Unless otherwise specified, the measurements shall be performed at a environmental temperature of 22±3°C.

For all measurements the nominal power supply, bias and clocking conditions apply. The nominal power supply and bias conditions are given in Table 14 on page 24, the timing diagrams in Figure 35 on page 51 and Figure 37 on page 53.

Remark: The given bias and power supply settings imply that the devices are measured in "soft- reset" condition.

5.5.2 Electrical and Electro-optical measurements at High and Low Temperature

The parameters to be measured to verify the electrical and electro-optical specifications are scheduled in Table 5 on page 15 and Table 6 on page 16. Unless otherwise specified, the measurements shall be performed at

-40 (-5 +0) °C and at +85 (+5 -0) °C.

5.5.3 Circuits for Electrical and Electro-optical Measurements

Circuits for performing the electro-optical tests in Table 4 on page 14 and Table 13 on page 24 are shown in Figure 48 on page 63 to Figure 51 on page 63.

5.6 Burn-in Test

5.6.1 Parameter Drift Values

The parameter drift values for power burn-in are specified in Table 7 on page 18 of this specification. Unless otherwise specified the measurements shall be conducted at a environmental temperature of 22±3°C and under nominal power supply, bias and timing conditions.

The parameter drift values shall not be exceeded. In addition to these drift value requirements, also the limit values of any parameter - as indicated in Table 4 on page 14 - shall not be exceeded.

Conditions for high temperature reverse bias burn-in

Not Applicable

5.6.2 Conditions for Power Burn-in

The conditions for power burn-in shall be as specified in Table 10 on page 21 of this specification

5.6.3 Electrical Circuits for High Temperature Reverse Bias Burn-in

Not Applicable

5.6.4 Electrical Circuits for Power Burn-in

Circuits to perform the power burn-in test are shown in Figure 48 on page 63 and next ones of this specification.

5.7 Environmental and Endurance Tests

5.7.1 Electrical and Electro-optical Measurements on Completion of Environmental Test

The parameters to be measured on completion of environmental tests are scheduled in Table 11 on page 21. Unless otherwise stated, the measurements shall be performed at a environmental temperature of 22±3°C. Measurements of dark current must be performed at 22±1°C and the actual environmental temperature must be reported with the test results.

5.7.2 Electrical and Electro-optical Measurements At Intermediate Point During Endurance Test

The parameters to be measured at intermediate points during endurance test of environmental tests are scheduled in Table 11 on page 21. Unless otherwise stated, the measurements shall be performed at an environmental temperature of 22±3°C

5.7.3 Electrical and electro-optical measurements on Completion of Endurance Test

The parameters to be measured on completion of endurance tests are scheduled in Table 11 on page 21. Unless otherwise stated, the measurements shall be performed at a environmental temperature of 22±3°C

5.7.4 Conditions for Operating Life Test

The conditions for operating life tests shall be as specified in Table 10 on page 21 of this specification.

5.7.5 Electrical Circuits for Operating Life Test

Circuits for performing the operating life test are shown in Figure 48 on page 63 and next ones of this specification.

5.7.6 Conditions for High Temperature Storage Test

The temperature to be applied shall be the maximum storage temperature specified in Table 2 on page 9 of this specification.

5.8 Total Dose Radiation Test

5.8.1 Application

The total dose radiation test shall be performed in accordance with the requirements of ESCC Basic specification 22900.

5.8.2 Parameter Drift Values

The allowable parameter drift values after total dose irradiation are listed in Table 8 on page 19. The parameters shown are valid after a total dose of 42KRad and 168h/100°C annealing.

5.8.3 Bias conditions

Continuous bias shall be applied during irradiation testing as shown in Figure 48 on page 63 and next ones of this specification.

5.8.4 Electrical and Electro-optical Measurements

The parameters to be measured, prior to, during and on completion of the irradiation are listed in Table 13 on page 24 of this specification. Only devices that meet the specification in Table 4 on page 14 of this specification shall be included in the test samples.

5.9 Lot Acceptance and Screening

This paragraph describes the Lot Acceptance Testing (LAT) and screening on the HAS FM devices. All tests on device level have to be performed on screened devices (see Table 5.9.6 on page 7).

5.9.1 Wafer Lot Acceptance

This is the acceptance of the silicon wafer lot. This has to be done on every wafer lot that will be used for the assembly of flight models.

Test	Test method	Number of devices	Test condition	Test location
Wafer processing data review	PID	NA	NA	CY
SEM	ESCC 21400	4 naked dies	NA	Test house
Total dose test	ESCC 22900	3 devices	42 krad : 1krad/h	ESTEC by CY
Endurance test	MIL-STD-883 Method 1005	6 devices	2000h at +125 C	Test House

Before and after total dose test and endurance test:

- Electrical measurements before and after at high, low and room temperature. Conform Table 4 on page 14 and Table 5 on page 15,Table 6 on page 16 of this specification.
- Visual inspection before and after
- Detailed electro optical measurements before and after

5.9.2 Glass Lot Acceptance

Transmission and reflectance curves that are delievered with each lot shall be compared with the specifications in Table , “Glass Lid Specification,” on page 10

3 glass lid shall be chosen randomly from the lot and will be measured in detail. All obtained results will be compared with Figure 5 on page 27.

5.9.3 Package lot acceptance

5 packages shall be chosen randomly from the lot and will be measured in detail. All obtained results will be compared with Figure 2 on page 25.

A solderability test is covered in the assembly lot acceptance tests (Table 5.9.4).

5.9.4 Assembly Lot Acceptance

Test	Test method	Number of devices	Test condition	Test location
Special assembly house in process control				Assembly House
Bond strength test	MIL-STD-883 method 2011	2	D	Assembly House
Assembly House Geometrical data review	Review	All		CY
Solder ability Terminal strength Marking permanence	MIL-STD883, method 2003 MIL-STD 883, method 2004 ESCC 24800	3	D	Test House
Geometrical measurements	PID	All		CY
Temperature cycling	MIL-STD 883, method 1010	5	Condition B 50 cycles -55°C/+125°C	Test House
Moisture resistance	JEDEC Std. Method A101-B		240h at 85°C/85%	Test House
DPA:				
Die shear test	MIL-STD-883 method 2019	4	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

Before and after the following tests are done:

- Electrical measurements conform Table 4 on page 14 of this specification
- Detailed visual inspection
- Fine leak test + Gross leak test

Fine- and gross-leak tests shall be performed using the following methods:

Fine Leak test: MIL-STD-883, Test Method 1014, Condition A

Gross Leak test: MIL-STD-883, Test Method 1014, Condition C

The required leak rate for fine leak testing is 5·10-7 atms. cm3/s

5.9.5 Periodic Testing

Test	Test method	Number of devices	Test condition	Test location
Mechanical Shock	MIL-STD 883, method 2002	2	B - 5 shocks, 1500g – 0,5ms – ½ sine, 6 axes	Test House
Mechanical Vibration	MIL-STD 883, method 2007	2	A - 4 cycles, 20g 80 to 2000 Hz, 0,06 inch 20 to 80 Hz, 3 axes	Test House
DPA:				
Die shear test	MIL-STD-883 method 2019	2	N/A	Test House
Bond pull test	MIL-STD-883 method 2011		All wires	Test House

Periodic testing is required every 2 years. Before and after the following tests are done:

- Electrical measurements conform Table 4 on page 14.
- Detailed visual inspection
- Fine leak test + Gross leak test

Fine- and gross-leak tests shall be performed using the following methods:

Fine Leak test: MIL-STD-883, Test Method 1014, Condition A

Gross Leak test: MIL-STD-883, Test Method 1014, Condition C

The required leak rate for fine leak testing is 5·10 7 atms. cm3/s

5.9.6 Screening

Nr.	Test	Test method	Number of devices	Test condition	Test location
1	HCRT Electrical measure-ments	001-53958	All	HT +85°C LT -40°C RT +25°C	CY
2	Visual inspection	001-49283 + ICD	All		CY
3	Die placement measurements	Cypress internal proc.	All		CY
4	XRAY	ESCC 20900	All		Test House
5	Stabilization bake	MIL-STD-883 method 1008	All	48h at 125°C	Test House
6	Fine leak test	MIL-STD-883 method 1014	All	A	Test House
7	Gross leak test	MIL-STD-883 method 1014	All	C	Test House
8	Temperature cycling	MIL-STD-883 method 1010	All	B - 10 cycles -55°C +125°C	Test House
9	Biased Burn-in	ICD	All	240h at +125°C.	CY
10	Mobile Particle Detection	MIL-STD-883 method 2020	All	A	Test House
11	Fine leak test	MIL-STD-883 method 1014	All	A	Test House
12	Gross leak test	MIL-STD-883 method 1014	All	C	Test House
13	HCRT Electrical measure-ments	001-53958	All	HT +85°C LT -40°C RT +25°C	CY
14	Final Visual Inspection	001-49283 + ICD	All		CY

6. Tables and Figures

6.1 Specification Tables

Table 1. Type Variant Summary

HAS2 Type Variants	Engineering samples (HHCES)	Flight model samples (HHCS)
Optical Quality (See "Optical quality - Definitions" on page 70.)		
Dead pixels	100	20
Bright pixels in FPN image	50	20
Bad pixels in PRNU image	150	50
Bad columns	5	0
Bad rows	5	0
Bright pixel clusters:		
2 adjacent bright pixels	25	2
4 or more adjacent bright pixels	10	0
DSNU defects @ 22 dec BOL	1200	1000
DSNU defects @ 22 dec EOL	1500	1250
Particle Contamination		
Fixed particles outside focal plane	N/A	N/A
Mobile particles > 20um	0	0
Fixed particles on focal plane > 20um	0	0
Mobile particles > 10um and < 20um	20	10
Fixed particles on focal plane > 10um and < 20um		
Particles < 10um	N/A	N/A
Wafer lot acceptance (section 5.9.1 on page 5)	NO	YES
Glass lot acceptance (section 5.9.2 on page 5)	NO	YES
Assembly lot acceptance (Table 5.9.4 on page 6)	NO	YES
Periodic testing (Table 5.9.5 on page 7)	NO	YES
Screening (Table 5.9.6 on page 7)	NO	YES
Calibration data	Optional	YES
Visual Inspection + particle mapping	Optional	YES

Table 2. Maximum Ratings

No	Characteristic	Min	Typ	Max	Unit	Remarks
1	Any supply voltage except VDD_RES	-0.5	3.3	+7.0	V	
2	Supply voltage at VDD_RES	-0.5	3.3	+5.0	V	3.3V for normal operation; up to 5V for increased full well capacity.
3	Voltage on any input terminal	-0.5	3.3	Vdd + 0.5	V	
4	Soldering temperature	NA	NA	260	°C	Hand soldering only; See section 1.6 on page 1 for soldering instructions
5	Operating temperature	-40	NA	+85	°C	
6	Storage temperature	-55	NA	+125	°C	

Table 3. Detailed Specification All Type Variants

General Characteristics						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Image sensor format	N/A	1024x 1024	N/A	pixels	
2	Pixel size	N/A	18	N/A	µm	
3	ADC resolution	N/A	12	N/A	bit	10 bit accuracy at 5 Msamples / sec

Silicon Particle Contamination Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Optical quality: Particle max size	N/A	N/A	20	um	See "Type Variant Summary" on page 8

Mechanical Specifications						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1a	Flatness of image area	NA	7.4	NA	µm	Peak-to-peak at 25 ± 3 °C Specified by the foundry over an entire 8" wafer
1b	Flatness of glass lid	NA	90	150	µm	Towards ceramic package
2	Mass	7.7	7.85	8.0	g	
3	Total thickness	3.2	3.3	3.4	mm	Package + epoxy + glass lid
4a	Die position, X offset	NA	NA	0.1	mm	Die in center of cavity
4b	Die position, Y offset	NA	NA	0.1	mm	Die in center of cavity
5	Die position, parallelism vs window Die position, parallelism vs backside	-0.1 0.1	0 0	0.1 0.1	mm	
6	Die position, Y tilt	-0.1	0	0.1	°	
7	Die position, X tilt	-0.1	0	0.1	°	
8	Die – window distance	0.25	0.3	0.35	mm	

Glass Lid Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1a	XY size	26.7 x 26.7	26.8 x 26.8	26.9 x 26.9	mm	
1b	Thickness	1.4	1.5	1.6	mm	
2a	Spectral range for optical coating of window	440	NA	1100	nm	
2b	Reflection coefficient for window	NA	<0.8	<1.3	%	Over bandwidth indicated in 2a
3	Optical quality: Scratch max width Scratch max number Dig max size Dig max number	N/A	N/A	 10 5 60 25	µm	

Environmental Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Operating temperature	-40	NA	+85	°C	
2	Storage temperature	-55	NA	+125	°C	Lower storage temperatures (to -80 deg C) have been tested and the device survives but this is not a fully qualified temperature.
3	Sensor total dose radiation tolerance	N/A	42	N/A	krad (Si)	Tested for functionality up to 300krad, 42 krad is guaranteed
4	sensor SEL threshold with ADC enabled	NA	NA	>110	MeV cm^3 mg^{-1}	Equivalent LET value

Electrical Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5MHz sampling rate Measured
3	Power supply current to ADC, operational: analog + digital	17	19	21	mA	ADC at 5MHz sampling rate Measured
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output amplifier voltage range	2.2	2.45	2.6	V	
8	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.30	1.35	1.40	V	
14	Output amplifier offset setting 32	0.43	0.51	0.6	V	
15	Output amplifier offset setting 63	0.80	0.90	1.0	V	
16	ADC ladder network resistance	NA	1.8	NA	kΩ	Typical value
17	ADC Differential non linearity	NA	7	11	lsb	
18	ADC Integral non linearity	NA	8	18	lsb	
19	ADC set-up time	5	NA	NA	ns	Analog_in stable to CLK_ADC rising
20	ADC hold time	10	NA	NA	ns	Analog_in stable after CLK_ADC rising edge
21	ADC delay time	NA	NA	20	ns	
22	ADC latency	NA	6.5	NA	-	Cycles of CLK_ADC
23	ADC ideal input range	0.85	NA	2.0	V	VLOW_ADC to VHIGH_ADC
24	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES=3.3V
25	Output range	0.8	NA	2.1	V	Measured with PGA in unity gain, offset=0.8V, low is dark, high is bright.
26	Linear range of pixel signal swing	40	50 0.75	NA	ke- V	Measured within ±1%
27	Linear range	60	82	NA	ke-	Measured within ±5%
28	Full well charge	90	100	NA	ke-	Measured with VDD_RES=3.3V
29	Quantum efficiency x Fillfactor	NA	45	NA	%	Measured between 500 nm and 650 nm. Refer to section 6.3.1 for complete curve.
30	Spectral response	NA	33.3	NA	%	Measured average over 400-900nm.

Electrical Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
31	Charge to voltage conversion factor	NA	16.9	NA	µV/e-	At pixel
32	Charge to voltage conversion factor	13	14.8	15.6	µV/e-	Measured at output SIGNAL_OUT, unity gain
33a	Temporal noise (Soft Reset)	NA	55	95	e-	Dark noise, with DR/DS, internal ADC
33b	Temporal noise (Hard Reset)	N/A	75	125	e-	Dark noise, with DR/DS, internal ADC
33c	Temporal noise (HTS Reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
34a	Temporal noise (NDR Soft reset)	NA	75	100	e-	
34b	Temporal noise (NDR Hard reset)	NA	75	100	e-	
34c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
35	ADC quantization noise	NA	7	NA	e-	
36a	Local fixed pattern noise standard deviation (Hard reset)	NA	110	160	e-	With DR/DS
36b	Local fixed pattern noise standard deviation (Soft reset)	NA	70	140	e-	With DR/DS
36c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS
37a	Global fixed pattern noise standard deviation (Hard reset)	NA	115	180	e-	With DR/DS
37b	Global fixed pattern noise standard deviation (Soft reset)	NA	90	140	e-	With DR/DS
37c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS
37d	Global fixed pattern noise standard deviation (NDR, Soft reset)	14	15	18	e-	With NDR/CDS and external ADC
37e	Local Column fixed pattern noise standard deviation (NDR, Soft reset)	14	15	18	e-	With NDR/CDS and external ADC
38	Average dark signal	NA	190	400	e-/s	At 25 ± 2 °C die temp, BOL see “Dark Current vs Temperature Model” on page 33
39	Average dark signal	NA	5550	8730	e-/s	At 25 ± 2 °C die temp, EOL (25 krad)
40	Dark signal temperature dependency	5	5.8	8	°C	Sensor temperature increase for doubled average dark current.
41	Local dark signal non uniformity standard deviation	NA	260	400	e-/s	At 25 ± 2 °C die temp, BOL 96% of BOL average
42	Global dark signal non uniformity standard deviation	N/A	275	500	e-/s	At 25 ± 2 °C die temp, BOL 96% of BOL average
43	Local photo response non uniformity, standard deviation	NA	0.8	1.0	%	Of average response
44	Global photo response non uniformity, standard deviation	NA	1.8	5	%	Of average response
45	MTF X direction	NA	0.35	NA	NA	At Nyquist measured
46	MTF Y direction	NA	0.35	NA	-	At Nyquist measured

Electrical Specification						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
47	Pixel to pixel crosstalk X direction	NA	9.8	NA	%	Of total source signal – see section 6.3.6 for 2-D plot
48	Pixel to pixel crosstalk Y direction	NA	9.8	NA	%	Of total Source signal – see section 6.3.6 for 2-D plot
49	Anti-blooming capability	200	1000	NA		Typical
50	Pixel rate	NA	5	10	MHz	
51	Temperature sensor transfer curve	NA	-4.64	NA	mV/°C	BOL
52	Temperature sensor output signal range, Min to Max (typical)	800	NA	1700	mV	BOL
53	Temperature sensor linearity	NA	3	NA	mV	BOL
54	Temperature sensor transfer curve	NA	-4.64	NA	mV/°C	EOL
55	Temperature sensor output signal range, Min to Max (typical)	800	NA	1700	NA	EOL
56a	Image lag (Soft reset)	NA	0.54	NA	-	Soft reset
56b	Image lag (Hard reset)	NA	-0.2	NA	-	Hard reset
56c	Image lag (HTS reset)	NA	-0.15	NA	-	HTS reset

Table 4. Electrical and Electro-optical Measurements at Room Temperature

Electrical and Electro-optical Measurements at Room Temperature 22°C						
No.	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analogue output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC Differential non linearity	N/A	7	11	lsb	
19	ADC Integral non linearity	N/A	8	18	lsb	
20	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES=3.3V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
22a	Temporal noise (Soft reset)	NA	55	95	e-	Dark noise, with DR/DS, internal ADC
22b	Temporal noise (Hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22c	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
23a	Temporal noise (NDR Soft reset)	NA	75	100	e-	
23b	Temporal noise (NDR Hard reset)	NA	75	100	e-	
23c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (Soft reset)	N/A	70	140	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (Hard reset)	NA	110	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS

Electrical and Electro-optical Measurements at Room Temperature 22°C						
No.	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
26a	Global fixed pattern noise standard deviation (Soft reset)	NA	90	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (Hard reset)	NA	115	180	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS
27	Average dark signal	NA	190	400	e-/s	At 25 ± 2 °C die temp
28	Local dark signal non uniformity standard deviation	NA	260	400	e-/s	At 25 ± 2 °C
29	Global dark signal non uniformity standard deviation	NA	275	500	e-/s	At 25 ± 2 °C
30	Local photo response non uniformity, standard deviation	NA	0.8	1.0	%	Of average response
31	Global photo response non uniformity, standard deviation	NA	1.8	5	%	Of average response
32a	Image lag (Soft reset)	NA	0.54	NA	-	
32b	Image lag (Hard reset)	NA	-0.2	NA	-	
32c	Image lag (HTS reset)	NA	-0.15	NA	-	

Table 5. Electrical and Electro-optical measurements at High Temperature

Electrical and Electro-optical Measurements at High Temperature +85°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	17	20	23	mA	
2	Total power supply current, operational	35	38	41	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analogue output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.7	4.0	4.3	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.0	7.5	8.0	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.89	0.94	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.36	1.42	V	
16	Output amplifier offset setting 32	0.43	0.53	0.63	V	
17	Output amplifier offset setting 63	0.83	0.93	1.03	V	
18	ADC Differential non linearity	NA	8	11	lsb	
19	ADC Integral non linearity	NA	10	18	lsb	

Electrical and Electro-optical Measurements at High Temperature +85°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
20	Saturation voltage output swing	1.20	1.52	NA	V	VDD_RES=3.3V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
22a	Temporal noise (Soft reset)	NA	66	110	e-	DR/DS
22b	Temporal noise (Hard reset)	NA	85	125	e-	DR/DS
22c	Temporal noise (HTS reset)	NA	73	110	e-	DR/DS
23a	Temporal noise (NDR Soft reset)	NA	200	400	e-	
23b	Temporal noise (NDR Hard reset)	NA	170	300	e-	
23c	Temporal noise (NDR HTS reset)	NA	65	125	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (Soft reset)	NA	82	160	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (Hard reset)	NA	95	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	100	160	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (Soft reset)	NA	80	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (Hard reset)	NA	97	160	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	115	300	e-	With DR/DS
27	Average dark signal	NA	41000	60000	e-/s	At +85 ± 2 °C die temp
28	Local dark signal non uniformity standard deviation	NA	2800	4000	e-/s	
29	Global dark signal non uniformity standard deviation	NA	3100	4500	e-/s	
30	Local photo response non uniformity, standard deviation	NA	0.74	1.0	%	Of average response
31	Global photo response non uniformity, standard deviation	NA	1.7	5	%	Of average response
32a	Image lag (Soft reset)	NA	-0.13	NA	-	Soft reset
32b	Image lag (Hard reset)	NA	-0.09	NA	-	Hard reset
32c	Image lag (HTS reset)	NA	-0.12	NA	-	HTS reset

Table 6. Electrical and Electro-optical measurements at Low Temperature

Electrical and Electro-optical Measurements at Low Temperature -40°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	16	18	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	

Electrical and Electro-optical Measurements at Low Temperature -40°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
8	Output impedance analogue output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC Differential non linearity	N/A	7	11	lsb	
19	ADC Integral non linearity	N/A	11	18	lsb	
20	Saturation voltage output swing	1.20	1.49	NA	V	VDD_RES=3.3V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
22a	Temporal noise (Soft reset)	NA	59	100	e-	DR/DS
22b	Temporal noise (Hard reset)	NA	77	125	e-	DR/DS
22c	Temporal noise (HTS reset)	NA	70	125	e-	DR/DS
23a	Temporal noise (NDR Soft reset)	NA	80	125	e-	
23b	Temporal noise (NDR Hard reset)	NA	80	125	e-	
23c	Temporal noise (NDR HTS reset)	NA	75	125	e-	
24	ADC quantization noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (Soft reset)	NA	70	140	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (Hard reset)	NA	90	140	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	100	160	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (Soft reset)	NA	70	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (Hard reset)	NA	95	140	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	120	180	e-	With DR/DS
27	Average dark signal	NA	3.3	10	e-/s	
28	Local dark signal non uniformity standard deviation	NA	6	20	e-/s	
29	Global dark signal non uniformity standard deviation	NA	8	30	e-/s	
30	Local photo response non uniformity, standard deviation	NA	0.8	1.0	%	Of average response measured
31	Global photo response non uniformity, standard deviation	NA	1.8	5	%	Of average response measured

Electrical and Electro-optical Measurements at Low Temperature -40°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
32a	Image lag	NA	0.6	NA	-	Soft reset
32b	Image lag	NA	0.2	NA	-	Hard reset
32c	Image lag	NA	-1.2	NA	-	HTS reset

Table 7. Parameter Drift Values for Burn In

Electrical and Electro-optical Measurements at Room Temperature +22°C					
No	**Characteristic**	**Typical Value**	**Max Drift**	**Unit**	**Remarks**
1	Total power supply current stand-by	18.5	2	mA	
2	Total power supply current, operational	37	3	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	19	2	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	15.5	2	mA	
5	Output impedance digital outputs	NA	20	W	
6	Output impedance analogue output	NA	20	W	
7	Output amplifier voltage range	2.45	0.3	V	
8	Output amplifier gain setting 0	1	N/A	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	2.1	0.2	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	4.1	0.4	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.7	0.6	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.93	0.1	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.35	0.1	V	
14	Output amplifier offset setting 32	0.51	0.1	V	
15	Output amplifier offset setting 63	0.90	0.1	V	
16	ADC Differential non linearity	7	2	lsb	
17	ADC Integral non linearity	8	2	lsb	
18	Saturation voltage output swing	1.49	0.2	V	VDD_RES=3.3V
19	Output range	NA	0.2	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
20a	Temporal noise (Soft reset)	55	+15	e-	Dark noise, with DR/DS, internal ADC
20b	Temporal noise (Hard reset)	75	+15	e-	DARK noise, with DR/DS, internal ADC
20c	Temporal noise (HTS reset)	65	+15	e-	Dark noise, with DR/DS, internal ADC
21a	Temporal noise (NDR Soft reset)	75	+15	e-	
21b	Temporal noise (NDR Hard reset)	75	+15	e-	
21c	Temporal noise (NDR HTS reset)	70	+15	e-	
22	ADC quantisation noise	7	NA	e-	
23a	Local fixed pattern noise standard deviation (Soft reset)	70	+15	e-	With DR/DS

Electrical and Electro-optical Measurements at Room Temperature +22°C					
No	**Characteristic**	**Typical Value**	**Max Drift**	**Unit**	**Remarks**
23b	Local fixed pattern noise standard deviation (Hard reset)	110	+15	e-	With DR/DS
23c	Local fixed pattern noise standard deviation (HTS reset)	95	+30	e-	With DR/DS
24a	Global fixed pattern noise standard deviation (Soft reset)	90	+15	e-	With DR/DS
24b	Global fixed pattern noise standard deviation (Hard reset)	115	+15	e-	With DR/DS
24c	Global fixed pattern noise standard deviation (HTS reset)	110	+50	e-	With DR/DS
25	Average dark signal	190	+50	e-/s	At 25 ± 2 °C die temp
26	Local dark signal non uniformity standard deviation	260	+50	e-/s	At 25 ± 2 °C
27	Global dark signal non uniformity standard deviation	275	+50	e-/s	At 25 ± 2 °C
28	Local photo response non uniformity, standard deviation	0.8	+0.1	%	Of average response
29	Global photo response non uniformity, standard deviation	1.8	+0.3	%	Of average response
30a	Image lag (Soft reset)	0.54	NA	-	
30b	Image lag (Hard reset)	-0.2	NA	-	
30c	Image lag (HTS reset)	-0.15	NA	-	

Table 8. Parameter Drift Values for Radiation Testing

Electrical and Electro-optical Measurements at Room Temperature +22°C					
No	**Characteristic**	**Typical Value**	**Max Drift**	**Unit**	**Remarks**
1	Total power supply current stand-by	18.5	2	mA	
2	Total power supply current, operational	37	3	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	19	2	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	15.5	2	mA	
5	Output impedance digital outputs	N/A	20	W	
6	Output impedance analogue output	N/A	20	W	
7	Output amplifier voltage range	2.45	0.2	V	
8	Output amplifier gain setting 0	1	N/A	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	2.1	0.2	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	4.1	0.3	-	Nominal 4 relative to setting 0
11	Output amplifier gain setting 3	7.7	0.5	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.93	0.1	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.35	0.1	V	
14	Output amplifier offset setting 32	0.51	0.1	V	
15	Output amplifier offset setting 63	0.90	0.1	V	

Electrical and Electro-optical Measurements at Room Temperature +22°C					
No	**Characteristic**	**Typical Value**	**Max Drift**	**Unit**	**Remarks**
16	ADC Differential non linearity	7	1	lsb	
17	ADC Integral non linearity	8	1	lsb	
18	Saturation voltage output swing	1.49	0.2	V	VDD_RES=3.3V
19	Output range	N/A	0.2	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
20a	Temporal noise (Soft reset)	55	+30	e-	Dark noise, with DR/DS, internal ADC
20b	Temporal noise (Hard reset)	75	+30	e-	Dark noise, with DR/DS, internal ADC
20c	Temporal noise (HTS reset)	65	+30	e-	Dark noise, with DR/DS, internal ADC
21a	Temporal noise (NDR Soft reset)	75	+40	e-	
21b	Temporal noise (NDR Hard reset)	75	+40	e-	
21c	Temporal noise (NDR HTS reset)	70	+40	e-	
22	ADC quantisation noise	7	NA	e-	
23a	Local fixed pattern noise standard deviation (Soft reset)	70	+200	e-	With DR/DS
23b	Local fixed pattern noise standard deviation (Hard reset)	110	+100	e-	With DR/DS
23c	Local fixed pattern noise standard deviation (HTS reset)	95	+100	e-	With DR/DS
24a	Global fixed pattern noise standard deviation (Soft reset)	90	+200	e-	With DR/DS
24b	Global fixed pattern noise standard deviation (Hard reset)	115	+100	e-	With DR/DS
24c	Global fixed pattern noise standard deviation (HTS reset)	110	+100	e-	With DR/DS
25	Average dark signal	190	+6000	e-/s	At 25 ± 2 °C die temp
26	Local dark signal non uniformity standard deviation	260	+1500	e-/s	At 25 ± 2 °C
27	Global dark signal non uniformity standard deviation	275	+1500	e-/s	At 25 ± 2 °C
28	Local photo response non uniformity, standard deviation	0.8	+0.1	%	Of average response
29	Global photo response non uniformity, standard deviation	1.8	+0.3	%	Of average response
30a	Image lag (Soft reset)	0.54	NA	-	
30b	Image lag (Hard reset)	-0.2	NA	-	
30c	Image lag (HTS reset)	-0.15	NA	-	

Table 9. Conditions for High Temperature Reverse Bias Burn-in

No	Characteristics	Symbol	Test condition	Unit
Not applicable				

Table 10. Conditions for Power Burn-in and Operating Life Tests

No	Characteristics	Symbol	Test condition	Unit
1	Ambient temp	Tamb	125	°C
2	All power supplies	Vdd	3.3	V
3	Bias conditions		See Figure 48 on page 63 and next ones	
4	Clock frequency		10	MHz

Table 11. Electrical and Electro-optical Measurements on Completion of Environmental Tests and at Intermediate Points and on Completion of Endurance Testing

Electrical and Electro-optical Measurements at Room Temperature +22°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5MHz sampling rate measured
3	Power supply current to ADC, operational	17	19	21	mA	at 5MHz
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Input impedance digital input	3	NA	NA	MΩ	
6	Input impedance ADC input	3	NA	NA	MΩ	
7	Output impedance digital outputs	NA	NA	400	W	
8	Output impedance analogue output	NA	NA	1	kΩ	
9	Output amplifier voltage range	2.2	2.45	2.6	V	
10	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
11	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
12	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0
13	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
14	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
15	Output amplifier offset setting 31	1.30	1.35	1.40	V	
16	Output amplifier offset setting 32	0.43	0.51	0.6	V	
17	Output amplifier offset setting 63	0.80	0.90	1.0	V	
18	ADC Differential non linearity	NA	7	11	lsb	
19	ADC Integral non linearity	NA	8	18	lsb	
20	Saturation voltage output swing	1.20	1.49	N/A	V	VDD_RES=3.3V
21	Output range	0.8	NA	2.1	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
22a	Temporal noise (Soft reset)	NA	55	95	e-	DARK noise, with DR/DS, internal ADC
22b	Temporal noise (Hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22c	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
23a	Temporal noise (NDR Soft reset)	NA	75	100	e-	
23b	Temporal noise (NDR Hard reset)	NA	75	100	e-	

Electrical and Electro-optical Measurements at Room Temperature +22°C						
No	**Characteristic**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
23c	Temporal noise (NDR HTS reset)	NA	70	100	e-	
24	ADC quantisation noise	NA	7	NA	e-	
25a	Local fixed pattern noise standard deviation (Soft reset)	NA	70	140	e-	With DR/DS
25b	Local fixed pattern noise standard deviation (Hard reset)	NA	110	160	e-	With DR/DS
25c	Local fixed pattern noise standard deviation (HTS reset)	NA	95	140	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (Soft reset)	NA	90	140	e-	With DR/DS
26b	Global fixed pattern noise standard deviation (Hard reset)	NA	115	180	e-	With DR/DS
26c	Global fixed pattern noise standard deviation (HTS reset)	NA	110	180	e-	With DR/DS
27	Average dark signal	NA	190	400	e-/s	At 25 ± 2 °C die temp
28	Local dark signal non uniformity standard deviation	NA	260	400	e-/s	At 25 ± 2 °C
29	Global dark signal non uniformity standard deviation	NA	275	500	e-/s	At 25 ± 2 °C
30	Local photo response non uniformity, standard deviation	NA	0.8	1.0	%	Of average response
31	Global photo response non uniformity, standard deviation	NA	1.8	5	%	Of average response
32a	Image lag (Soft reset)	NA	0.54	NA	-	
32b	Image lag (Hard reset)	NA	-0.2	NA	-	
32c	Image lag (HTS reset)	NA	-0.15	NA	-	

Table 12. Electrical and Electro-optical Measurements during and on Completion of Total-dose Irradiation Testing (50krad)

Electrical and Electro-optical Measurements at Room Temperature +22°C						
No	**Characteristic Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
1	Total power supply current stand-by	16	18.5	21	mA	
2	Total power supply current, operational	35	37	40	mA	ADC at 5MHz sampling rate
3	Power supply current to ADC, operational	17	19	21	mA	ADC at 5MHz sampling rate
4	Power supply current to image core, operational	14	15.5	17	mA	
5	Output impedance digital outputs	NA	NA	400	W	
6	Output impedance analogue output	NA	NA	1	kΩ	
7	Output amplifier voltage range	2.2	2.45	2.6	V	
8	Output amplifier gain setting 0	NA	1	NA	-	Nominal 1 measured reference
9	Output amplifier gain setting 1	1.9	2.1	2.3	-	Nominal 2 relative to setting 0
10	Output amplifier gain setting 2	3.8	4.1	4.4	-	Nominal 4 relative to setting 0

Electrical and Electro-optical Measurements at Room Temperature +22°C						
No	**Characteristic Symbol**	**Min**	**Typ**	**Max**	**Unit**	**Remarks**
11	Output amplifier gain setting 3	7.2	7.7	8.2	-	Nominal 8 relative to setting 0
12	Output amplifier offset setting 0	0.86	0.93	1.0	V	0 decodes to middle value
13	Output amplifier offset setting 31	1.30	1.35	1.40	V	
14	Output amplifier offset setting 32	0.43	0.51	0.6	V	
15	Output amplifier offset setting 63	0.80	0.90	1.0	V	
16	ADC Differential non linearity	N/A	8	11	lsb	
17	ADC Integral non linearity	N/A	9	18	lsb	
18	Saturation voltage output swing	1.20	1.49	N/A	V	VDD_RES=3.3V
19	Output range	0.8	N/A	2.1	V	PGA in unity gain, offset=0.8V, low is dark, high is bright.
20	Temporal noise (Soft reset)	NA	55	95	e-	Dark noise, with DR/DS, internal AD
21	Temporal noise (Hard reset)	NA	75	125	e-	Dark noise, with DR/DS, internal ADC
22a	Temporal noise (HTS reset)	NA	65	110	e-	Dark noise, with DR/DS, internal ADC
22b	Temporal noise (NDR Soft reset)	NA	75	100	e-	
22c	Temporal noise (NDR Hard reset)	NA	75	100	e-	
23a	Temporal noise (NDR HTS reset)	NA	70	100	e-	
23b	ADC quantization noise	NA	7	NA	e-	
23c	Local fixed pattern noise standard deviation (Soft reset)	NA	70	350	e-	With DR/DS
24	Local fixed pattern noise standard deviation (Hard reset)	NA	110	160	e-	With DR/DS
25a	Local fixed pattern noise standard deviation (HTS reset)	NA	95	200	e-	With DR/DS
25b	Global fixed pattern noise standard deviation (Soft reset)	NA	90	350	e-	With DR/DS
25c	Global fixed pattern noise standard deviation (Hard reset)	NA	115	180	e-	With DR/DS
26a	Global fixed pattern noise standard deviation (HTS reset)	NA	110	200	e-	With DR/DS
26b	Average dark signal	NA	5550	8730	e-/s	At 25 ± 2 °C die temp
26c	Local dark signal non uniformity standard deviation	NA	260	2000	e-/s	At 25 ± 2 °C
27	Global dark signal non uniformity standard deviation	NA	275	2000	e-/s	At 25 ± 2 °C
28	Local photo response non uniformity, standard deviation	NA	0.8	1.0	%	Of average response
29	Global photo response non uniformity, standard deviation	NA	1.8	5	%	Of average response
30	Image lag (Soft reset)	NA	0.54	NA	-	
31	Image lag (Hard reset)	NA	-0.2	NA	-	
32a	Image lag (HTS reset)	NA	-0.15	NA	-	

Table 13. Electro-optical Measurements on the Optical Bench

No	Characteristic Symbol	Min	Typ	Max	Unit	Remarks
1	Linear range of pixel signal swing	40	50 0.75	NA	ke- V	Measured within ±1%
2	Linear range	60	82	NA	ke-	Measured within ±5%
3	Full well charge	90	100	NA	ke-	Measured VDD_RES=3.3V
4	Quantum efficiency x Fillfactor	NA	45	NA	%	Measured between 500 nm and 650 nm. Refer to "Specification Figures" on page 25 for complete curve
5	Spectral Response	NA	33.3	-	%	Measured average over 400-900nm.
6	Charge to voltage conversion factor	NA	16.9	-	µV/e-	at pixel
7	Charge to voltage conversion factor	13	14.8	15.6	µV/e-	Measured at output SIGNAL_OUT, unity gain
8	MTF X direction	NA	0.35	NA	-	at Nyquist measured
9	MTF Y direction	NA	0.35	NA	-	at Nyquist measured
10	Pixel to pixel crosstalk X direction	NA	9.8	NA	%	of total source signal – see "Specification Figures" on page 25 for 2-D plot
11	Pixel to pixel crosstalk Y direction	NA	9.8	NA	%	of total source signal – see "Specification Figures" on page 25 for 2-D plot
12	Anti-blooming capability	NA	1000	NA	Ke-	predicted value

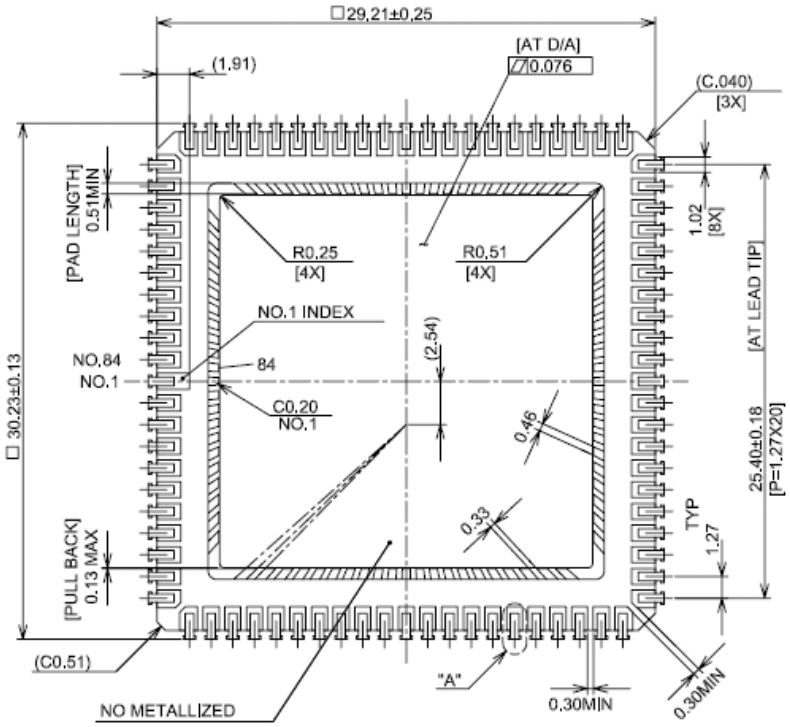
Table 14. Typical Power Supply Settings and Sensor Settings

Power Supply Settings	
ADC_VLOW	0.85V
ADC_VHIGH	2.0V
V_ADC_DIGITAL	3.3V
V_ADC_ANALOG	3.3V
VDDD	3.3V
VDDA	3.3V
VRES	3.3V for SR / 4.2V for HR
VPIX	3.3V (for HTS switched to 0.75V)

Sensor Settings	
Read Out Modes	Destructive – Non Destructive
Integration Time	195 us
Gain Setting	Unity
Offset Setting	0
X Clock Period	100ns

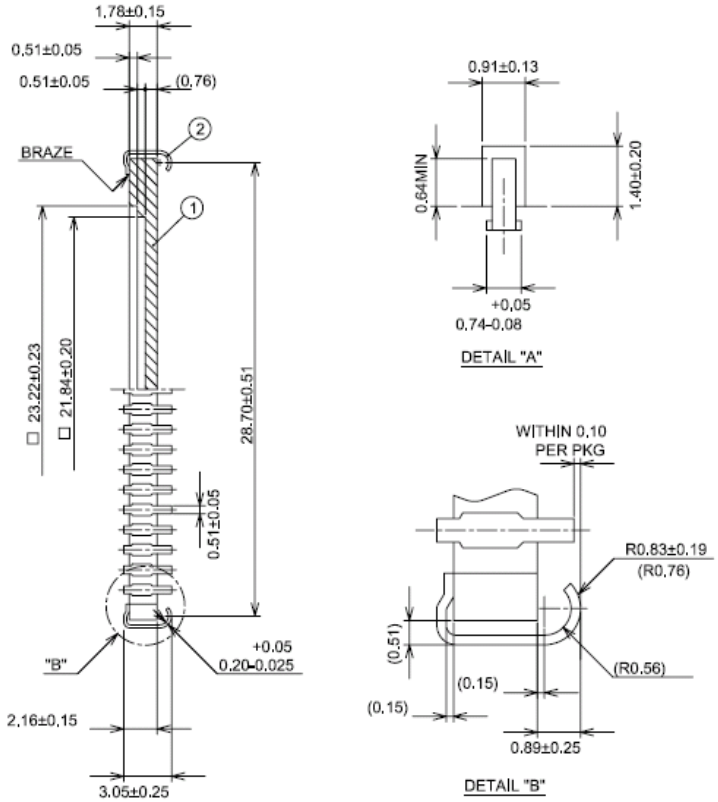
6.2 Specification Figures

Figure 1. 84L JLCC Package



001-07594**

Figure 2. Physical and Geometrical Package Drawings



001-07594**

Figure 3. HAS2 Assembled Device Side View

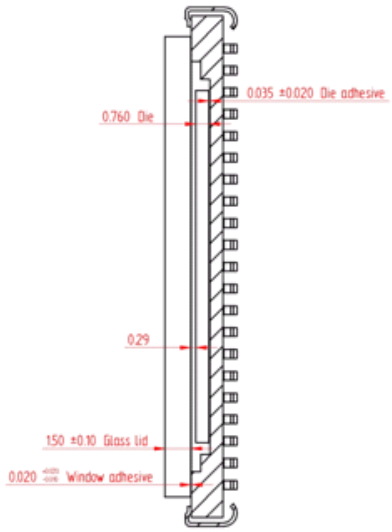


Figure 4. Die Placement Dimensions

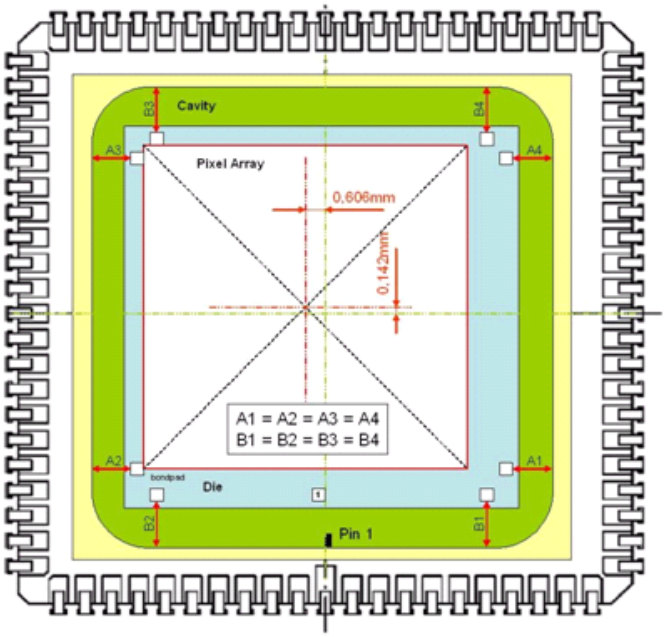


Figure 5. Glass Lid Dimensions

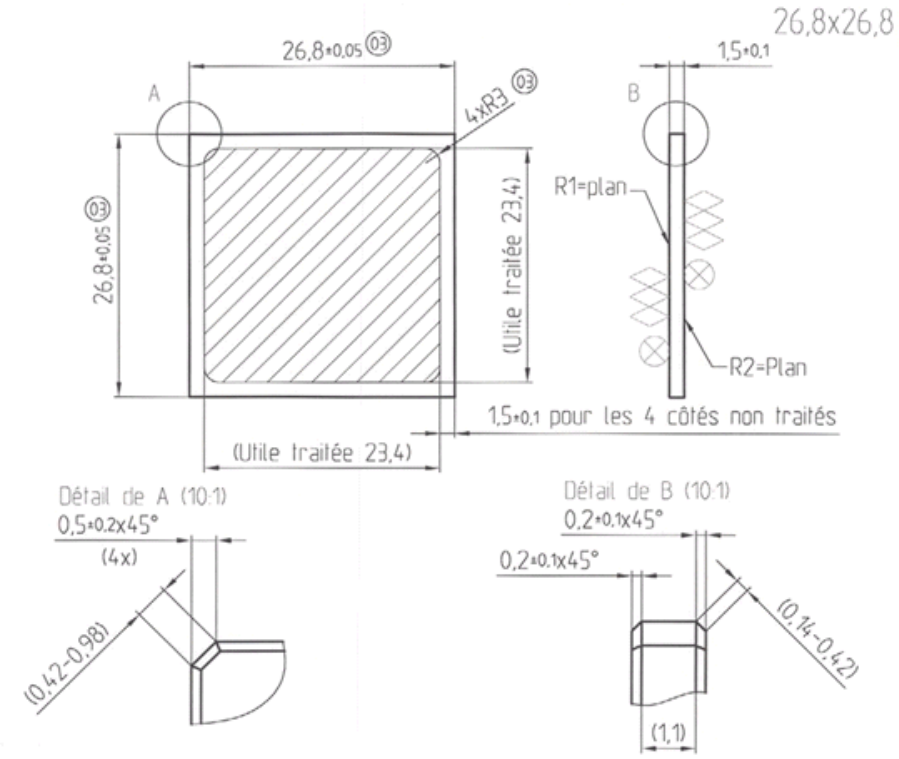


Figure 6. Pin Assignment

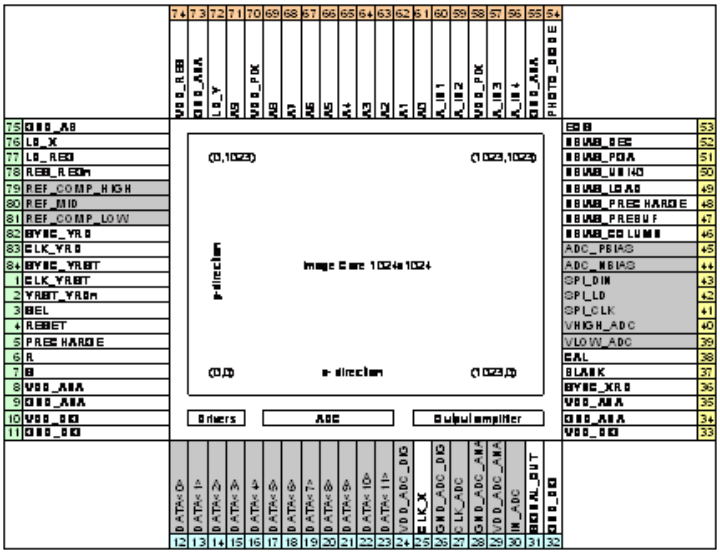
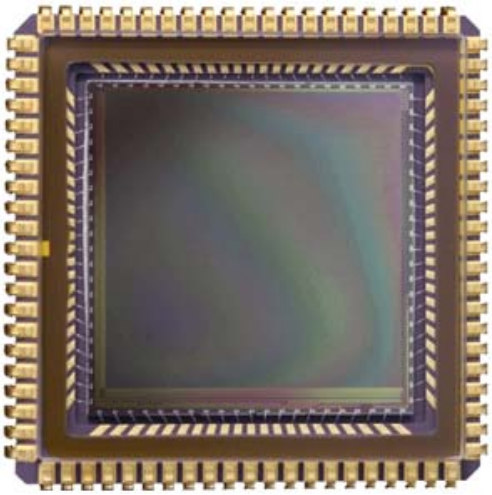


Figure 7. HAS2 Physical Layout



6.3 Typical data

6.3.1 Spectral Response

Figure 8. Measured Spectral Response of HAS Rad-hard Pixel. Black Curve indicates Average Spectral Response

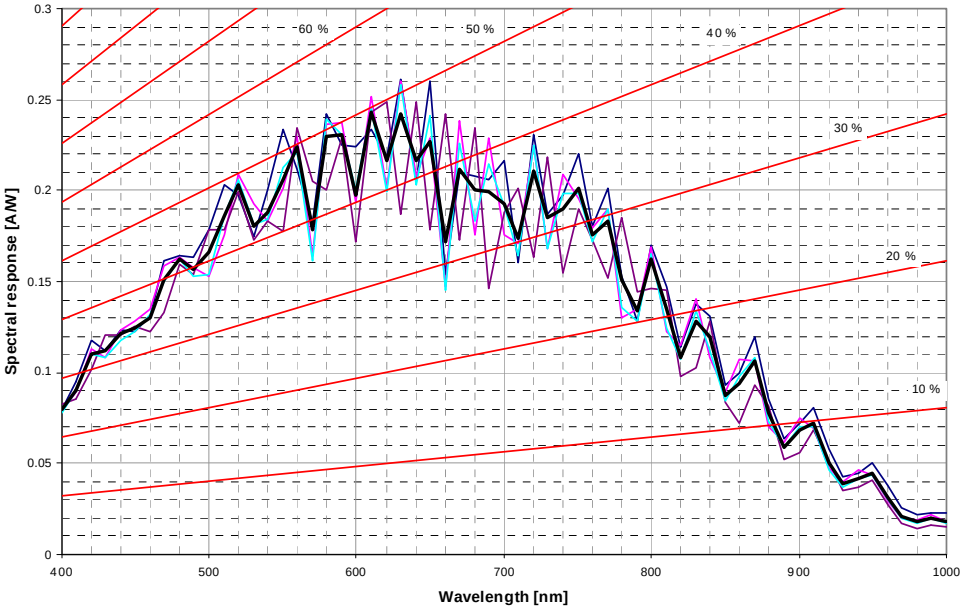
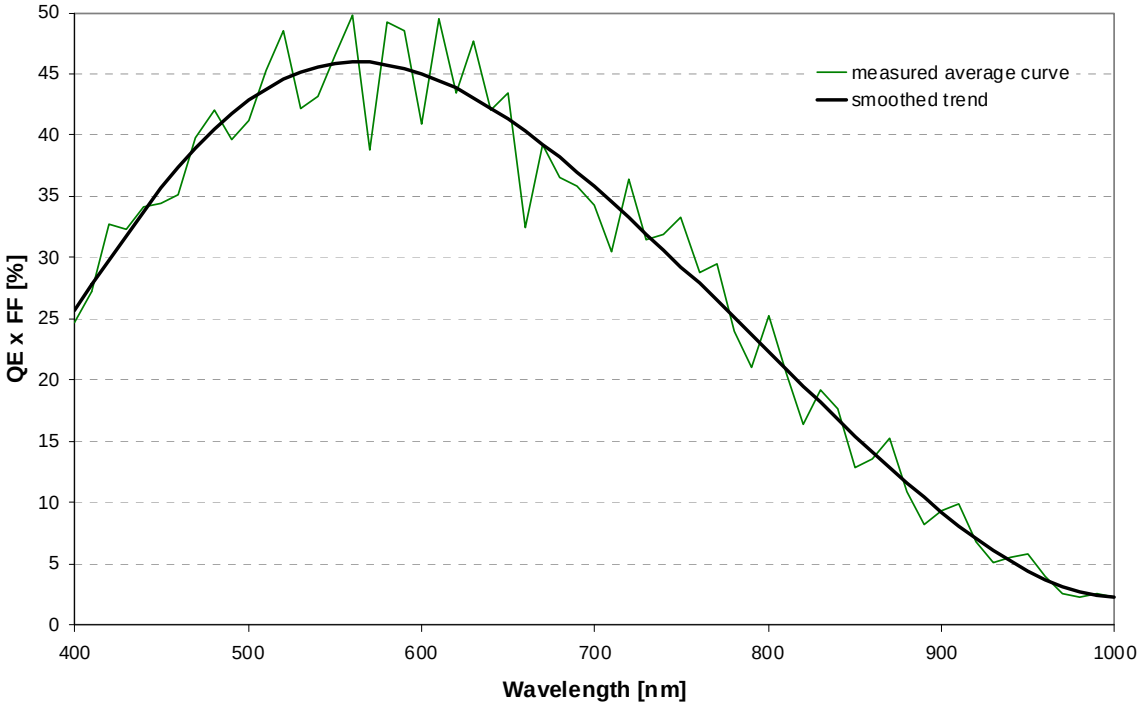
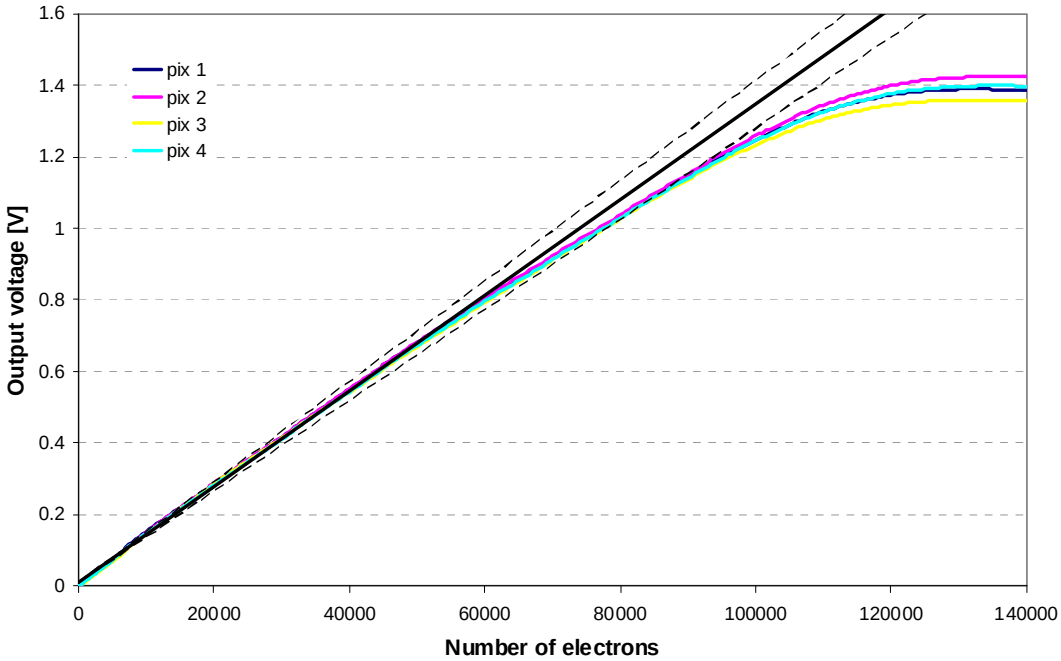


Figure 9. Average Measured Spectral Response of HAS Rad-hard Pixel Recalculated to QExFF



6.3.2 Photo-response Curve

Figure 10. Pixel Response Curve: Photo-electrons versus Signal Voltage



Fit to the linear response curve with the same conversion gain (solid black line). The dashed lines indicate linear response curves with -5% and +5% conversion gain

A detailed analysis is performed in the range < 4000 e-. The dashed lines corresponds to soft reset. The others to hard reset.

Figure 11. Pixel Response Curve < 4000e-

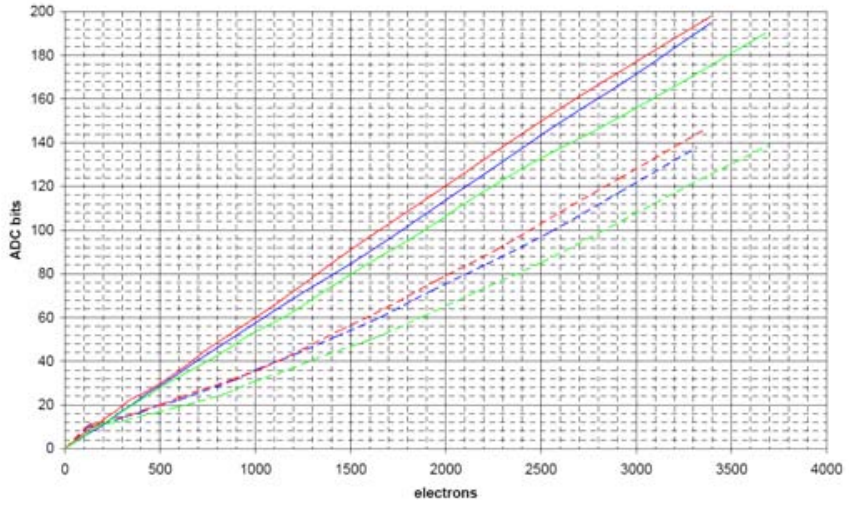


Figure 12. Measured Response Curves of Two Pixels on Two Devices at different Gain Setting

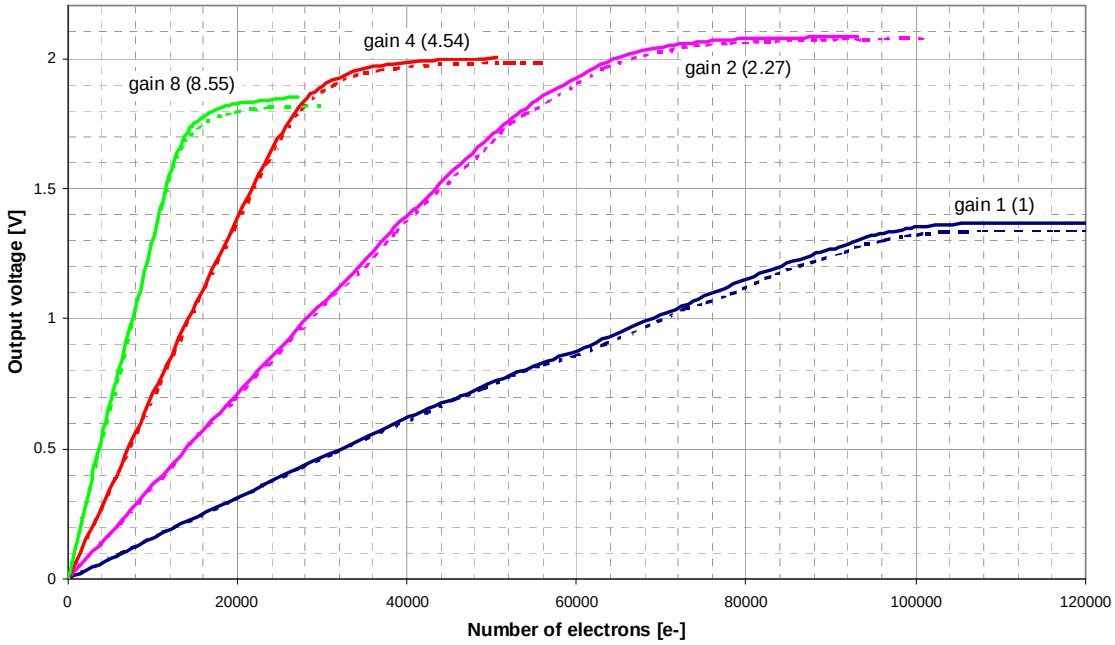


Table 15. Overview of the Offset at different Gain Settings

	Device	1	6	Average	Average
Gain setting	Offset	[V]	[V]	[V]	Offset drift [mV]
1	offset_g1	0.86	0.85	0.86	0
2	offset_g2	0.93	0.91	0.92	65
4	offset_g4	1.02	0.99	1.00	149
8	offset_g8	1.18	1.14	1.16	303

6.3.3 Fixed Pattern Noise

Figure 13 shows a log linear plot of the fixed pattern noise in destructive readout before and after radiation.

Figure 13. Typical FPN Histogram in DR Before and After TID

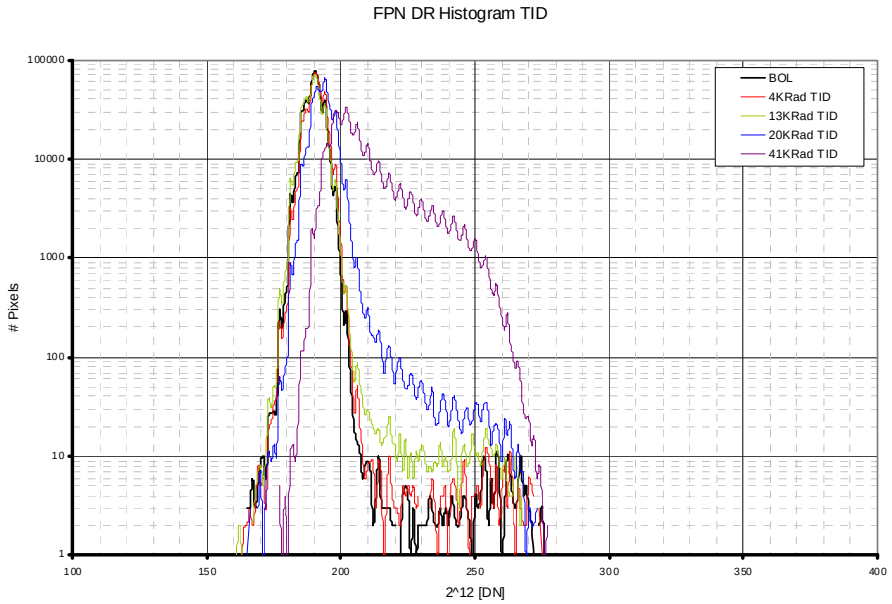


Figure 12 on page 30 shows a log linear plot of the fixed pattern noise in destructive readout before and after a 2000h life test which can be considered as EOL 41ehavior.

Figure 14. Fpn Histogram in DR before and after 2000h Life Test

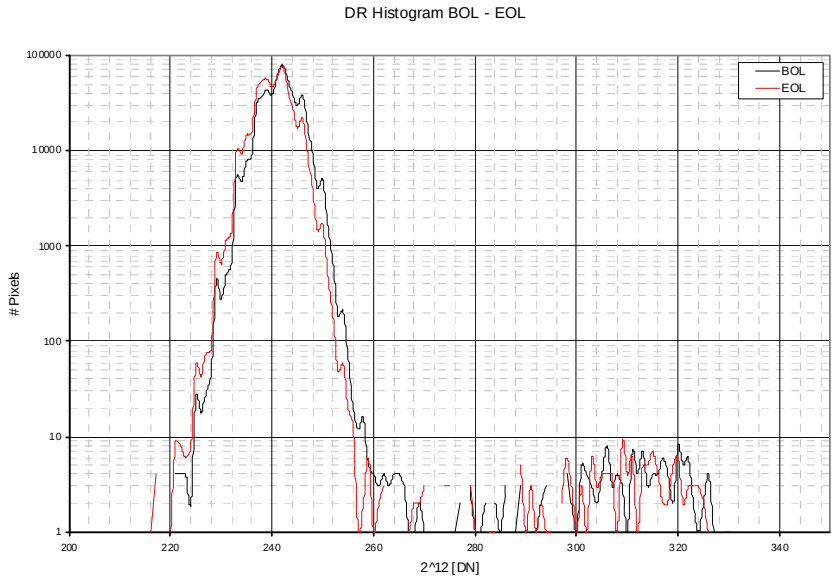
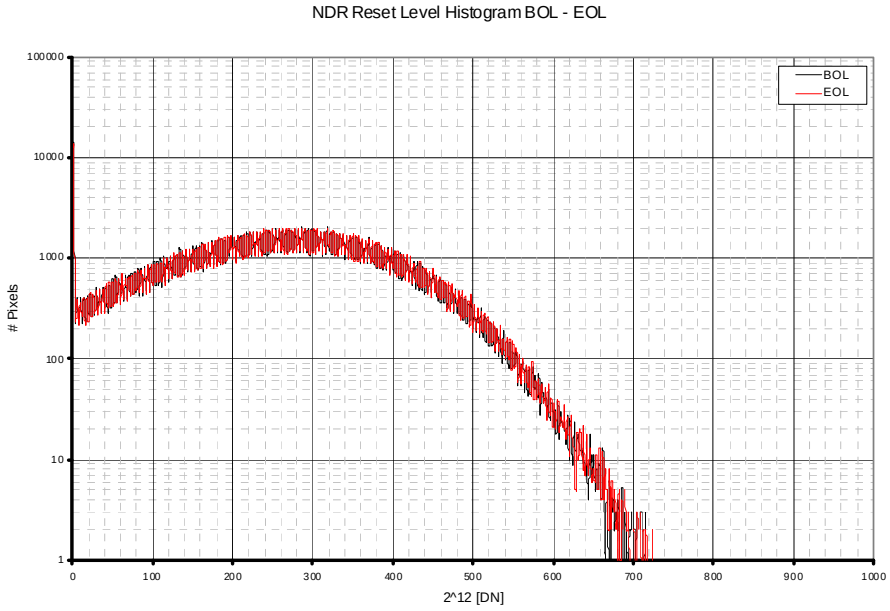


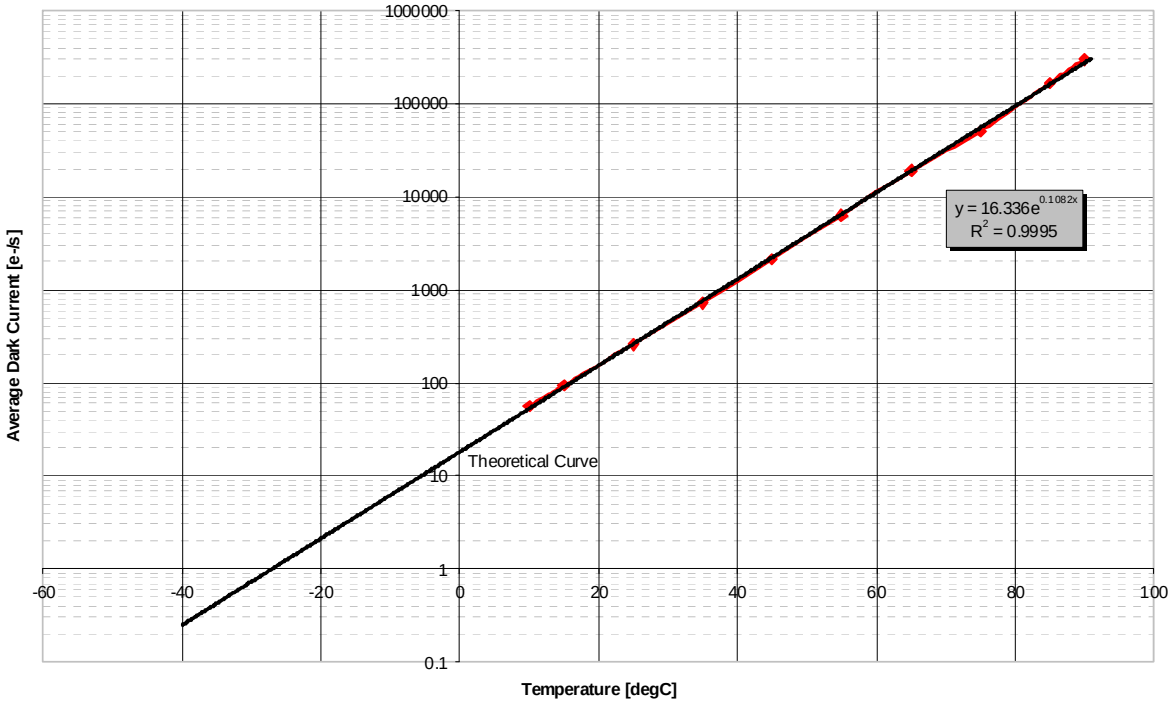
Figure 15 shows a log linear plot of the fixed pattern noise in non destructive readout before and after a 2000h life test which can be considered as EOL 42ehavior.

Figure 15. FPN Histogram in NDR before and after 2000h Life test



6.3.4 Dark Current vs Temperature Model

Figure 16. Temperature Dependence of the Dark Current (in e/s) Measured on a Sample



Following model is consistent with what has been measured for typical values:

$$DC = DC_0\, 2^{\frac{T-T_0}{\Delta T_{DC,d1}}} + a_{DC}\, TID\, 2^{\frac{T-T_0}{\Delta T_{DC,d2}}}$$

$$DCNU = DCNU_0\, 2^{\frac{T-T_0}{\Delta T_{DCNU,d1}}} + a_{DCNU}\, TID\, 2^{\frac{T-T_0}{\Delta T_{DCNU,d2}}}$$

with

DC the dark current in e/s

DC0 the dark current at 30 °C and 0 krad = 300 e/s

TID the total ionizing dose (in krad(Si))

T the temperature (in °C)

aDC the slope of the curve at 30 °C = 325 e/s/krad(Si)

ΔTDC,d1 = 5.8 °C and ΔTDC,d2 = 7.1 °C

DCNU0 the dark current non-uniformity at 30 °C and 0 krad = 230 e/s

aDCNU the slope of the curve at 30 °C = 33.6 e/s/krad(Si)

ΔTDCNU,d1 = 9.5 °C and ΔTDCNU,d2 = 9.5 °C

T0 = 30 °C

Following model is consistent with what has been measured for **worst case** values:

$$DC = DC_0\ 2^{\frac{T-T_0}{\Delta T_{DC,d1,L}}} + a_{DC}\ TID\ 2^{\frac{T-T_0}{\Delta T_{DC,d2,L}}} \quad \text{for T < T0}$$

$$DC = DC_0\ 2^{\frac{T-T_0}{\Delta T_{DC,d1,H}}} + a_{DC}\ TID\ 2^{\frac{T-T_0}{\Delta T_{DC,d2,H}}} \quad \text{for T > T0}$$

$$DCNU = DCNU_0\ 2^{\frac{T-T_0}{\Delta T_{DCNU,d1,L}}} + a_{DCNU}\ TID\ 2^{\frac{T-T_0}{\Delta T_{DCNU,d2,L}}} \quad \text{for T < T0}$$

$$DCNU = DCNU_0\ 2^{\frac{T-T_0}{\Delta T_{DCNU,d1,H}}} + a_{DCNU}\ TID\ 2^{\frac{T-T_0}{\Delta T_{DCNU,d2,H}}} \quad \text{for T > T0}$$

with

DC the dark current in e/s

DC0 the dark current at 30 °C and 0 krad = 550 e/s

TID the total ionizing dose (in krad(Si))

T the temperature (in °C)

aDC the slope of the curve at 30 °C = 480 e/s/krad(Si)

ΔTDC,d1,L = 6.6 °C and ΔTDC,d2,L = 8 °C for T < T0

ΔTDC,d1,H = 5 °C and ΔTDC,d2,H = 6.5 °C for T > T0

DCNU0 the dark current non-uniformity at 30 °C and 0 krad = 400 e/s

aDCNU the slope of the curve at 30 °C = 45 e/s/krad(Si)

ΔTDCNU,d1,L = 10.5 °C and ΔTDCNU,d2,L = 10.5 °C for T < T0

ΔTDCNU,d1,H = 8.5 °C and ΔTDCNU,d2,H = 8.5 °C for T > T0

T0 = 30 °C

DCNU Distributions

Figure 17 and Figure 18 show the distributions of the dark current in mV/s and e/s respectively for a number of devices and the average distribution.

Figure 17. Dark Current Distribution (in mV/s) at 25 ºC Ambient Temperature

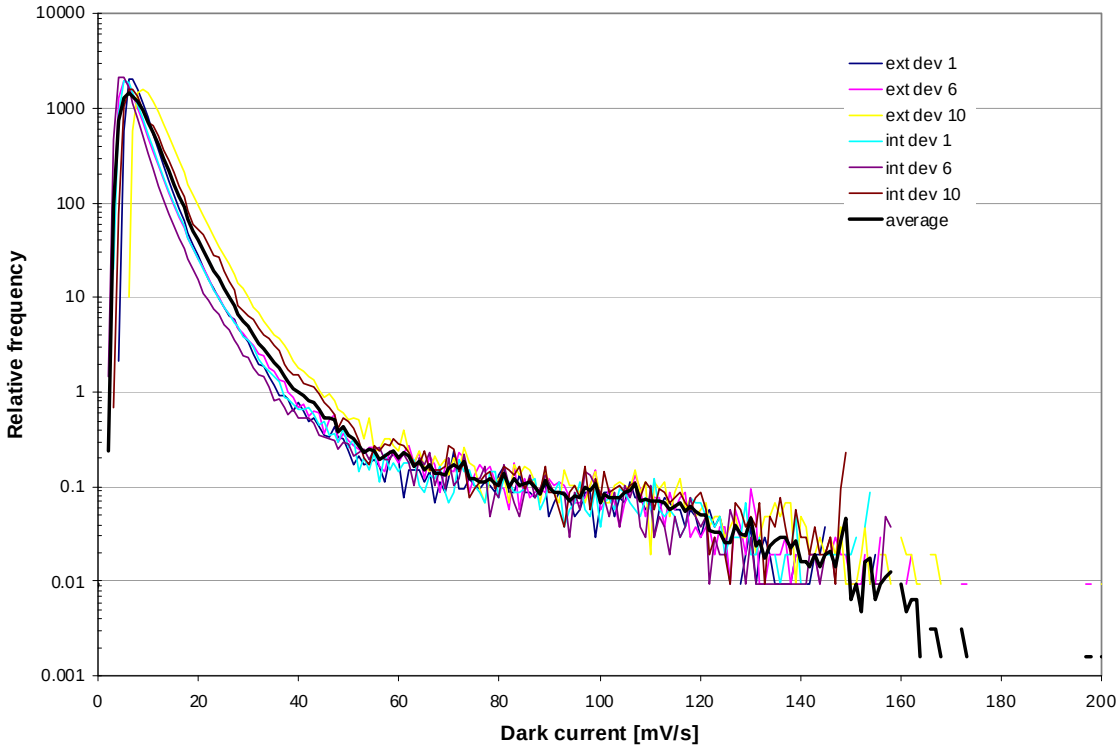


Figure 18. Dark Current Distribution (in e/s) at 25 ºC Ambient Temperature

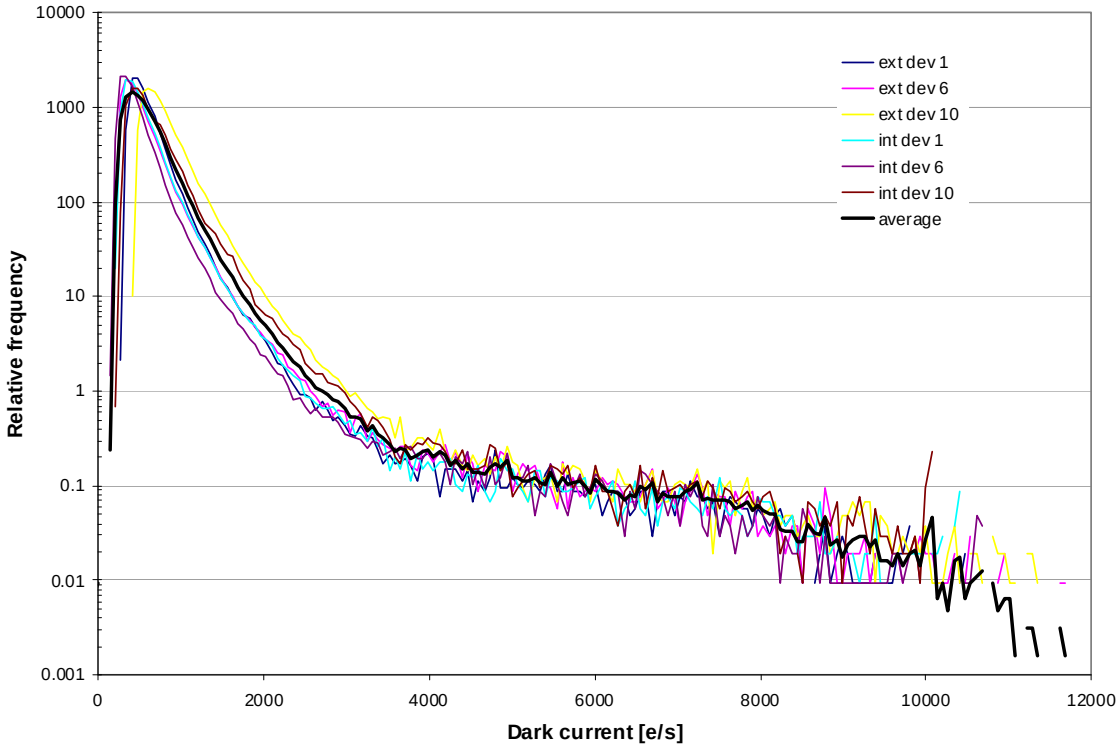


Figure 19 and Figure 20 show the cumulative distributions of the dark current in mV/s and e/s respectively for a number of devices and the average cumulative distribution.

Figure 19. Cumulative Dark Current Distribution (in mV/s) at 25 ºC Ambient Temperature

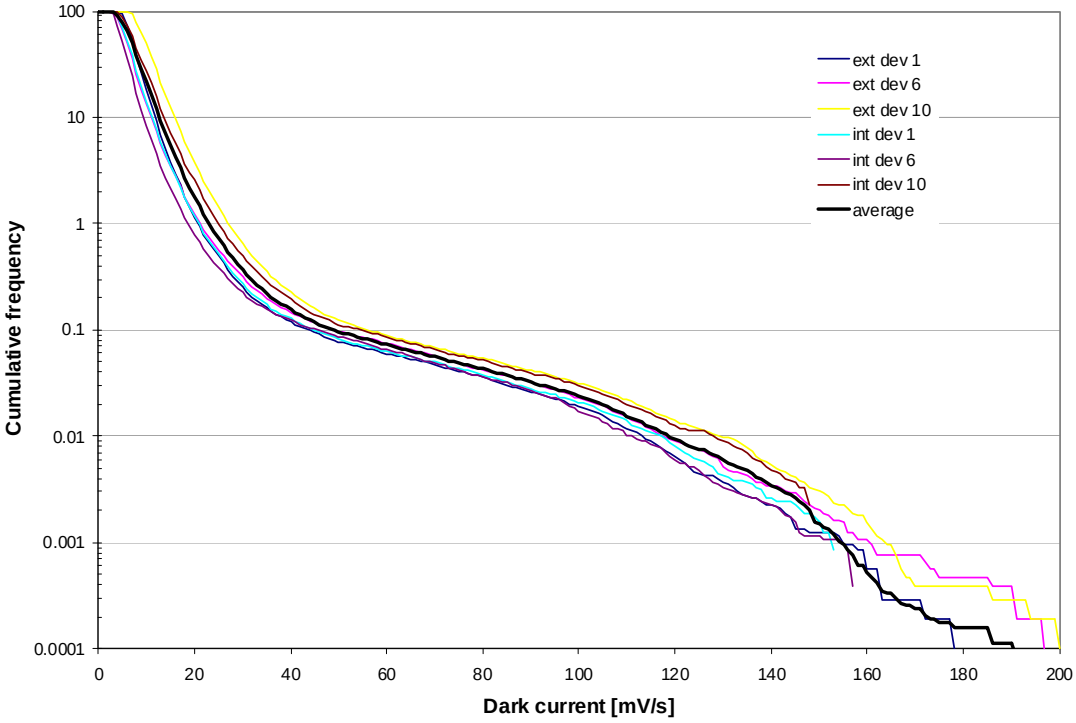


Figure 20. Cumulative Dark Current Distribution (in e/s) at 25 ºC Ambient Temperature

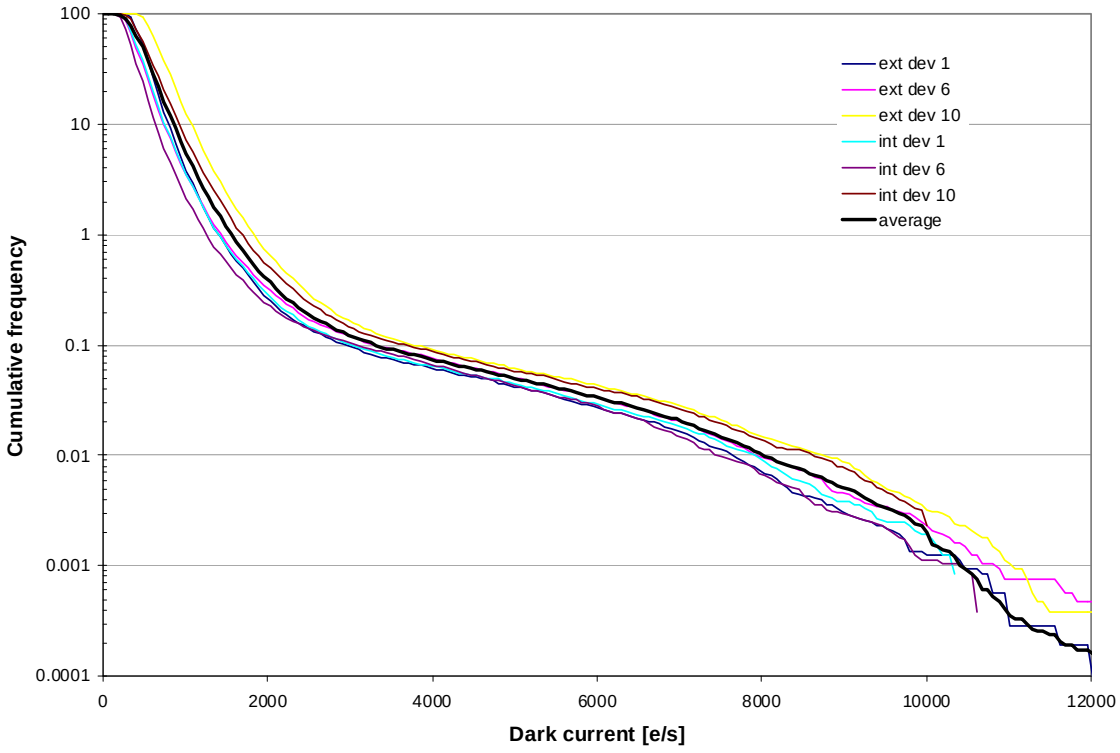


Figure 21 shows the percentage of pixels versus their normalized dark current for the measurement and for a Gaussian distribution with the same average value and standard deviation. In the measured distribution, about 1.1-1.2 % of the pixels exhibit a dark current that exceeds the 3σ limit that is typically used to exclude pixels from the measurements (about 10 times larger than for Gaussian distribution).

Figure 21. Comparison between Measured Distribution and Gaussian Distribution

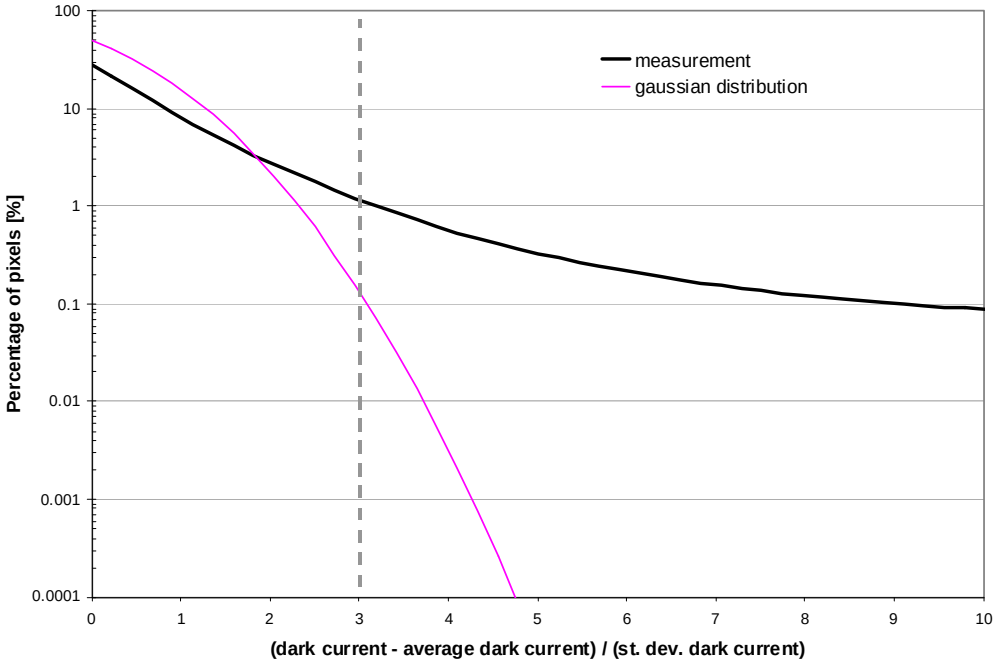
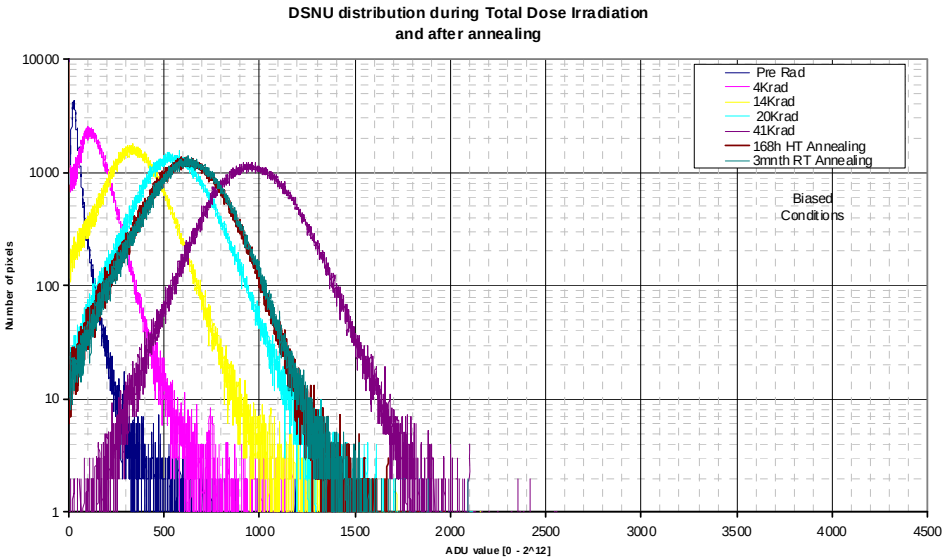


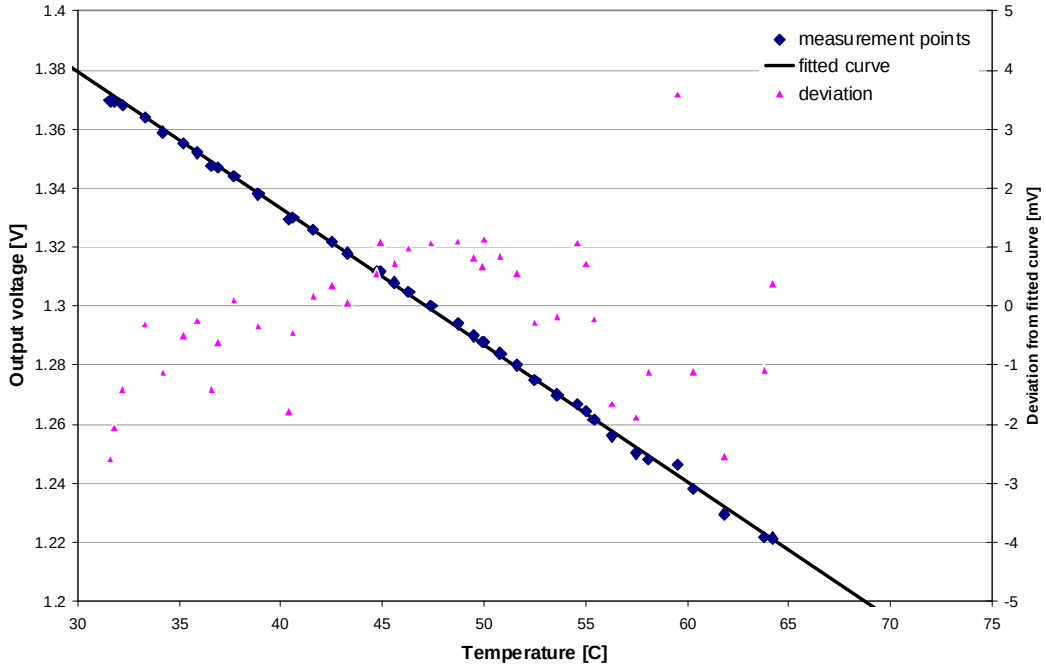
Figure 22 shows the DSNU distributions during TID irradiation

Figure 22. DSNU Distributions during TID Irradiation



6.3.5 Temperature Sensor

Figure 23. Temperature Sensor Voltage Sensitivity: The solid line indicates a linear fit with 1.38 V as output voltage at 30 ºC and a slope of -4.64 mV/ºC



6.3.6 Pixel-to-Pixel Cross Talk

Figure 24. Cross talk with central pixel uniformly illuminated with 100 %. Estimation from Knife-edge measurements

0.0	0.2	1.3	0.2	0.0
0.2	1.3	9.8	1.3	0.2
1.3	9.8	**49.0**	9.8	1.3
0.2	1.3	9.8	1.3	0.2
0.0	0.2	1.3	0.2	0.0

7. Pin Description

7.1 Pin Type Information

The following conventions are used in the pin list.

Pin Types	
AI	Analogue Input
AO	Analogue Output
AB	Analogue Bias
DI	Digital Input
DO	Digital Output
VDD	Supply Voltage
GND	Supply Ground

7.2 Power Supply Considerations

It is suggested to use one regulator for all digital supply pins together, one regulator for the sensor core analogue supplies together, and one regulator for the ADC analogue supply (if used). Analogue ground returns must be of very low impedance, as short-term peaks of 200mA can be encountered.

The ADC can be disabled by connecting all of its power and ground pins to system ground, leaving all other pins open.

7.3 Pin List

Doubled-up pins have the same pin name, but are indicated with (*). These pins are at the same potential on the chip.

Pin No.	Name	Type	Purpose
Power Supply and Ground Connections			
10	VDD_DIG (1)	VDD	Logic power, 3.3V
33	VDD_DIG (2)	VDD	
11	GND_DIG (1)	GND	Logic ground
32	GND_DIG (2)	GND	
8	VDD_ANA (1)	VDD	Analogue power, 3.3V
35	VDD_ANA (2)	VDD	
9	GND_ANA (1)	GND	Analogue ground
34	GND_ANA (2)	GND	
55	GND_ANA (3)	GND	
73	GND_ANA (4)	GND	
58	VDD_PIX (1)	VDD	Pixel array power, 3.3V
70	VDD_PIX (2)	VDD	
74	VDD_RES	VDD	Reset power, 3.3V, optionally up to 5V for increased full well
Sensor Biasing			
75	GND_AB	AB	Antiblooming ground, connect to system ground or to a low-impedant 1V source for enhanced anti-blooming
52	NBIAS_DEC	AB	Connect with 200kΩ to VDD_ANA, decouple with 100nF to GND_ANA
51	NBIAS_PGA	AB	Connect with 200kΩ to VDD_ANA, decouple with 100nF to GND_ANA

Pin No.	Name	Type	Purpose
50	NBIAS_UNI40	AB	Connect with 75kΩ to VDD_ANA, decouple with 100nF to GND_ANA
49	NBIAS_LOAD	AB	Connect to GND_ANA
48	NBIAS_PRECHARGE	AB	Connect with 110kΩ to VDD_ANA, decouple with 100nF to GND_ANA
47	NBIAS_PREBUF	AB	Connect with 200kΩ to VDD_ANA, decouple with 100nF to GND_ANA
46	NBIAS_COLUMN	AB	Connect with 110kΩ to VDD_ANA, decouple with 100nF to GND_ANA
Analog Signal Input and Outputs			
31	SIGNAL_OUT	AO	Output of PGA, range ## .. ## V, straight polarity i.e. a low output voltage corresponds to a dark pixel reading.
60	A_IN1	AI	Input to PGA input multiplexer.
59	A_IN2	AI	Input to PGA input multiplexer.
57	A_IN3	AI	Input to PGA input multiplexer.
56	A_IN4	AI	Input to PGA input multiplexer.
54	PHOTODIODE	AO	Reference photodiode
Logic Control Inputs and Status Outputs			
71	A9	DI	Parallel sensor programming interface shared address/data bus, MSB
69	A8	DI	
68	A7	DI	
67	A6	DI	
66	A5	DI	
65	A4	DI	
64	A3	DI	
63	A2	DI	
62	A1	DI	
61	A0	DI	Parallel sensor programming interface shared address/data bus, LSB
72	LD_Y	DI	Load strobe: copy A[9..0] into Y1 start register
76	LD_X	DI	Load strobe: copy A[9..0] into X1 start register
77	LD_REG	DI	Load strobe: copy A[7..0] into parameter register indicated by A[9..8]
78	RES_REGn	DI	Asynchronous reset for internal registers
82	SYNC_YRD	DI	Initialise Y read shift register (YRD) to position indicated by Y1 start register
84	SYNC_YRST	DI	Initialise Y reset shift register (YRST) to position indicated by Y1 start register
36	SYNC_XRD	DI	Initialise X read shift register (XRD) to position indicated by X1 start register
83	CLK_YRD	DI	Advance shift register YRD one position
1	CLK_YRST	DI	Advance shift register YRST one position

Pin No.	Name	Type	Purpose
25	CLK_X	DI	Advance shift register XRD; note: two clock cycles needed for one pixel output
53	EOS	DO	End Of Scan monitor output for YRD,YRST,XRD shift registers, selected through an internal register
2	YRST_YRDn	DI	Enable YRD to address the pixel array when ‘0’; Enable YRST to address the pixel array when ‘1’
4	RESET	DI	Reset the line pointed to by YRST (YRST_YRDn=’1’) or pointed to by YRD (YRST_YRDn=’0’)
37	BLANK	DI	Assert when in line blanking / non-readout phase
3	SEL	DI	Select for readout the line pointed to by YRST (YRST_YRDn=’1’) or YRD (YRST_YRDn=’0’)
5	PRECHARGE	DI	Precharge column bus
6	R	DI	Sample the selected line’s levels onto the column amplifier reset level bus
7	S	DI	Sample the selected line’s levels onto the column amplifier signal level bus
38	CAL	DI	Calibrate PGA
ADC			
30	IN_ADC	AI	Analogue input to ADC
27	CLK_ADC	DI	ADC conversion clock, pixel rate, latency is 6.5 cycles
23	DATA_11	DO	ADC data output, MSB
22	DATA_10	DO	
21	DATA_9	DO	
20	DATA_8	DO	
19	DATA_7	DO	
18	DATA_6	DO	
17	DATA_5	DO	
16	DATA_4	DO	
15	DATA_3	DO	
14	DATA_2	DO	
13	DATA_1	DO	
12	DATA_0	DO	ADC data output, LSB
43	SPI_DIN	DI	Serial calibration interface data in
42	SPI_LD	DI	Serial calibration interface load strobe
41	SPI_CLK	DI	Serial calibration interface bit clock
44	ADC_NBIAS	AB	Connect with 60 kOhm resistor to ADC_PBIAS, decouple with 100nF to ground
45	ADC_PBIAS	AB	Connect with 60 kOhm resistor to ADC_NBIAS, decouple with 100nF to VDD_ADC_ANA
39	VLOW_ADC	AI	ADC low threshold reference voltage, connect with 90 Ohm to GND and 130 Ohm to VHIGH_ADC, decouple with 100nF to ground
40	VHIGH_ADC	AI	ADC high threshold reference voltage, connect with 130 Ohm to VDD_ANA_ADC, decouple with 100nF to ground
81	REF_COMP_LOW	AO	Decouple with 100nF to ground
80	REF_MID	AO	Decouple with 100nF to ground

Pin No.	Name	Type	Purpose
79	REF_COMP_HIGH	AO	Decouple with 100nF to ground
29	VDD_ADC_ANA	VDD	Analogue supply, 3.3V
28	GND_ADC_ANA	GND	Analogue ground
24	VDD_ADC_DIG	VDD	Digital supply, 3.3V
26	GND_ADC_DIG	GND	Digital ground

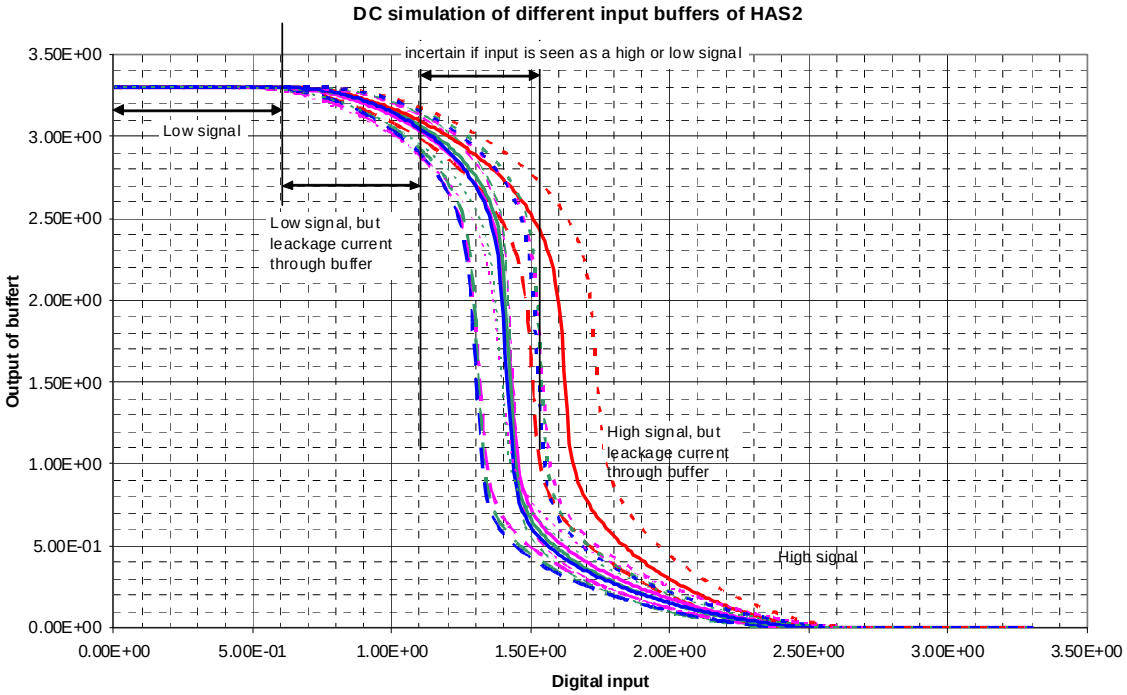
7.4 Electrical Characteristics

7.4.1 Multiplexer Inputs

Pin nr.	Name	Imput impedance	Settling Time
60	A_IN1	Capacitive 10pF	100ns
59	A_IN2	Capacitive 10pF	100ns
57	A_IN3	Capacitive 10pF	100ns
56	A_IN4	Capacitive 10pF	100ns

7.4.2 Digital I/O

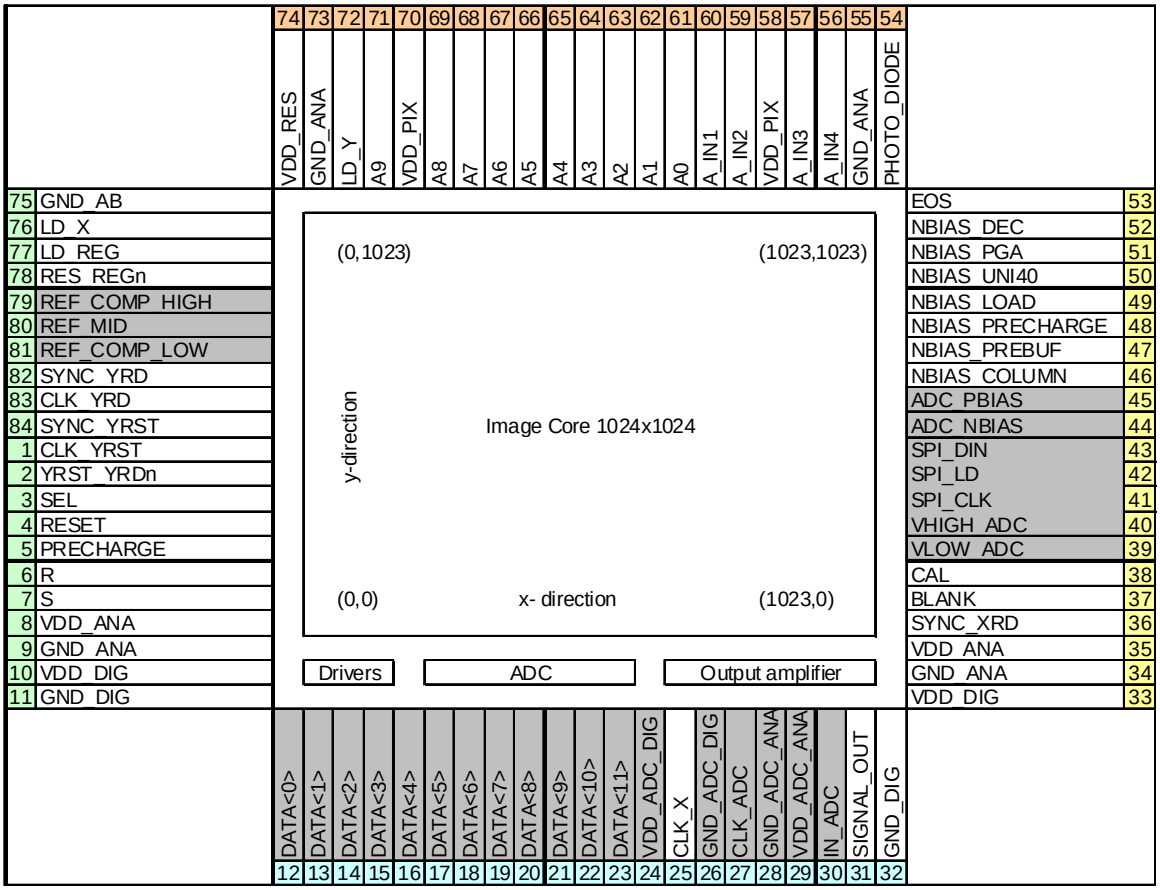
Figure 25. Simulation results Digital "0" and Digital "1"



7.5 Package Pin Assignment

The HAS sensor is packaged in a 84 pins JLCC84 package with large cavity. The figure below shows the pin configuration.

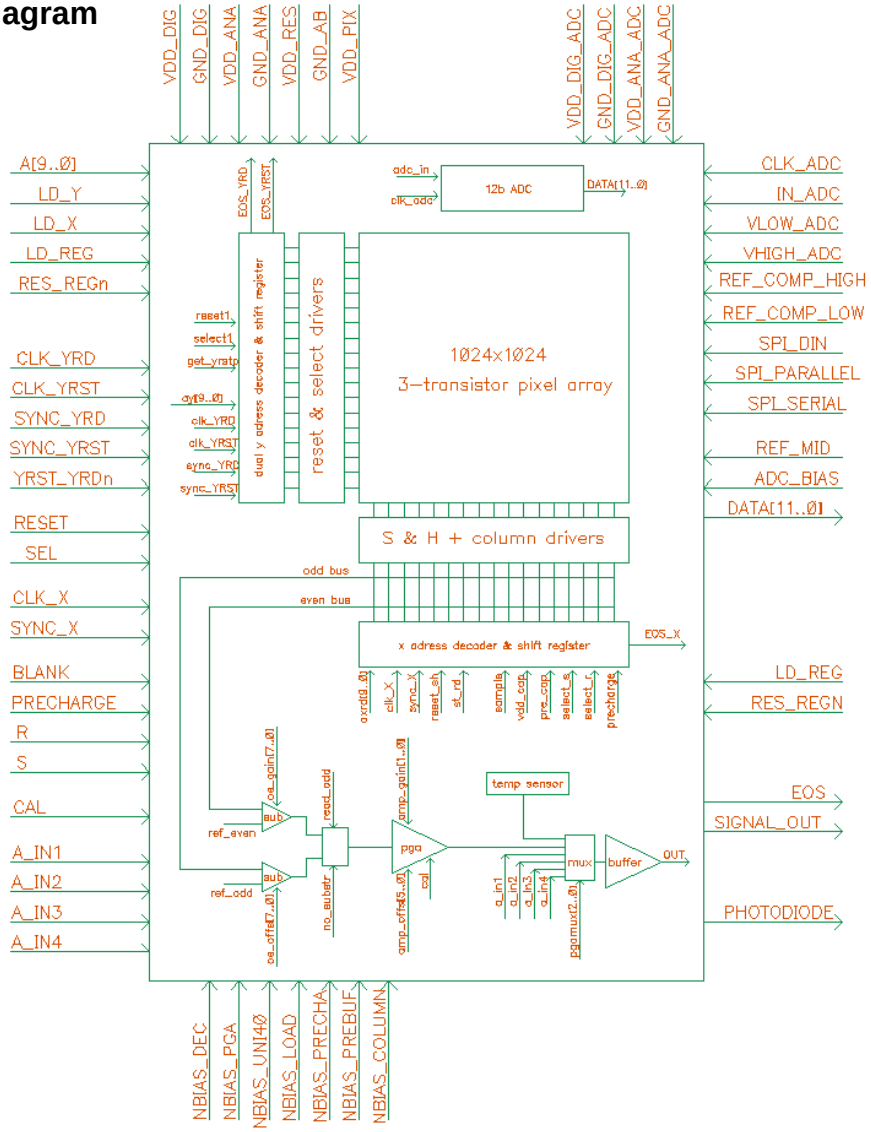
Figure 26. Pin Configuration



8. User Manual

8.1 Image Sensor Architecture

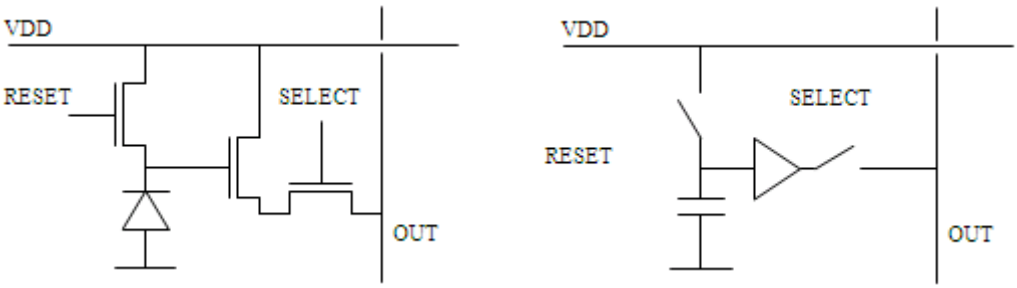
Sensor Block Diagram



8.1.1 Pixel Architecture

A square array contains 1024x1024 three-transistor linearly-integrating pixels of each 18 x 18 µm. Each pixel has a connection for a reset line, for power, an output select line, and eventually the pixel's output signal

Figure 27. Three-transistor Pixe: Transistor-level Diagram (left), and Functional Equivalent (right)



There are three transistors in a pixel. The first one acts as a switch between the power supply and the photodiode. The photodiode is equivalent to a capacitor with a light-controlled current source. The second transistor is a source follower amplifier, buffering the voltage at the photodiode/capacitor cathode for connection to the outside world. The third transistor again is a switch, connecting the output of the buffer amplifier to an output signal bus.

Activating the reset line drains the charges present on the pixel's embedded photodiode capacitor, corresponding to a black, dark, pre-exposure state, or high voltage. As all pixels on a row (line) share their reset control lines, the pixels in a row can only be reset together.

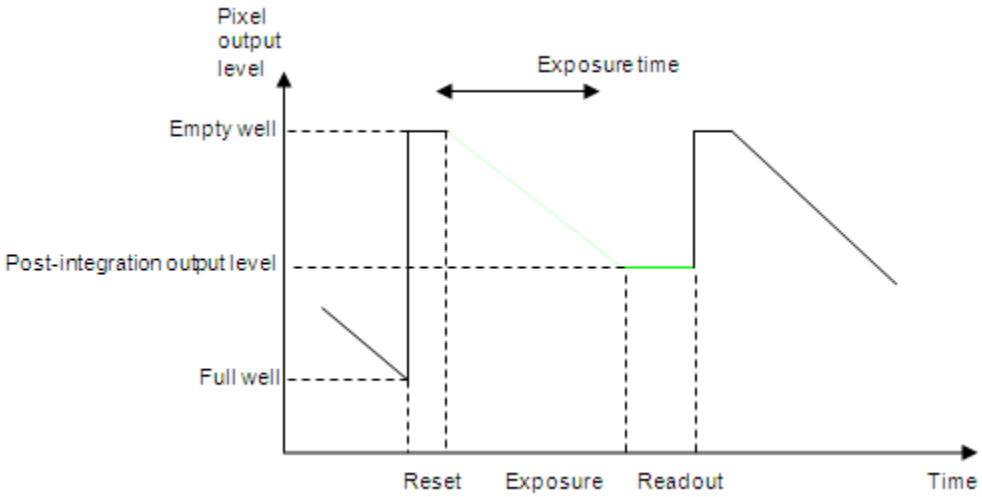
With both reset and select lines disabled the pixel amasses photo charges on its capacitor, charges generated in the photo-diode by impinging photons. During this integration the voltage on the photodiode cathode decreases.

When the select line is asserted the voltage on the capacitor is connected to the pixel output through the source follower buffer transistor.

All pixels in a line have their select lines tied together: upon selection a whole line of pixel output signals is driven onto the 1024 column buses that lead into the column amplifiers for further processing and complete or partial sequential readout to the ADC.

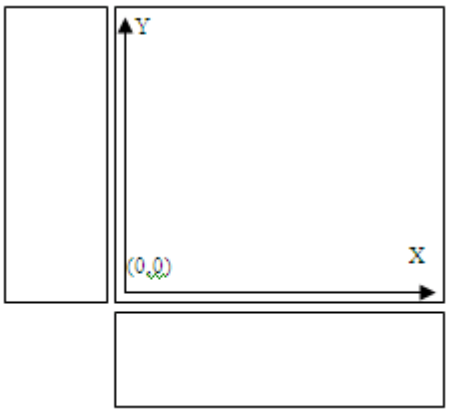
All pixels on a line have their reset lines tied together: the reset mechanism works on all pixels in a line simultaneously, no individual or addressed pixel reset (IPR) is possible.

Figure 28. Signal Lifetime in a Three-transistor Pixel: Reset to black level (high voltage), Photo Charge Integration (dropping voltage), voltage readout



8.1.2 Array Coordinate System

Figure 29. Front View of Sensor Die: Package pin 1 is on the left side. The focal plane origin is in the bottom-left corner. Lines (Y) are scanned down to top, pixels (X) left to right



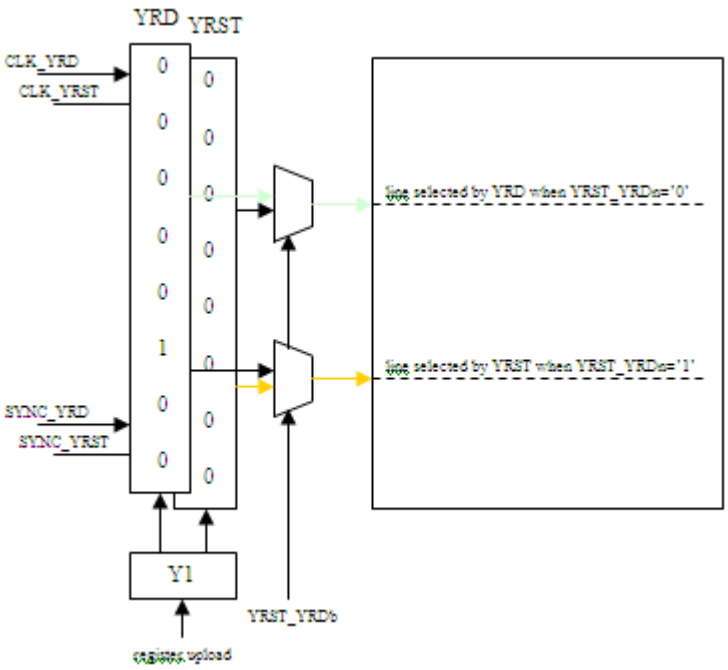
8.1.3 Line Addressing

The sensor operates line wise: a line of pixels can be selected and reset, and a line of pixels can be selected for readout into the column amplifier structures. There is no frame reset operation, there is no frame transfer.

Image acquisition is done by sequencing over all lines of interest and applying the required reset and/or readout control to each line selected.

The sensor array contains two vertical shift registers for line addressing. These registers are one-hot, i.e. they contain a pattern like "00001000000", at each time pointing to one line of pixels.

Figure 30. Line Addressing Structures: YRD and YRST one-hot shift register pointers and Y1 programmable start-of-scan register



In Double Sampling / Destructive readout, one of these registers is typically dedicated to addressing the lines to read, and the other is used for addressing the lines to reset as part of the electronic shutter operation.

In Correlated Double Sampling / Non-Destructive Readout, it is the user's choice whether one or both shift registers will be used.

Both Y shift registers can be initialized to a position indicated by an on-chip address register. This address register is written by the user through the parallel sensor programming interface. With this programmable initial position windowed readout (region-of-interest) is possible.

Both registers can be advanced one position at a time under user control.

8.1.4 Pixel Addressing

Pixels are read from left to right, generating a pixel-sequential output signal for each line. The pixel addressing is similar to the line addressing.

Close to the column amplifiers resides a horizontal shift register for pixel/column addressing. This register is one-hot, i.e. it contains a pattern like "00001000000", at a time pointing to exactly one pixel and one column amplifier.

Line acquisition is done by sequencing over all pixels of interest and applying each time the required pixel readout and ADC control signals.

The X shift register can be initialized to a position indicated by an on-chip address register. This address register is written by the user through the parallel sensor programming interface. With this programmable initial position windowed readout (region-of-interest) is possible. The X register can be advanced one position under user control. This requires a pixel clock signal at twice the frequency of the desired pixel rate.

8.1.5 Column Amplifiers

At the bottom of each column of pixels sits one column amplifier, for sampling the addressed pixel's signal and reset levels. These signals are then locally hold until that particular pixel is sent to the output channel, in this case PGA, multiplexer, buffer, and ADC.

The combination of column amplifiers and PGA can perform Double Sampling: in this case a pixel's signal level is read into the structures, then the pixel is reset, then the reset level is read into the structures and subtracted from the previously-stored signal level, cancelling fixed pattern noise.

In Correlated Double Sampling mode the column amplifiers are used in bypass mode, and the raw signal level (which can be either a dark reset level or a post-illumination signal level) is sent to the output amplifier, and then to the output for storage and correlated subtraction off-chip. This cancels fixed pattern noise as well as temporal KTC noise.

8.1.6 Input Signal Multiplexer

An analogue signal multiplexer with six inputs connects a number of sources to the output buffer.

One input always is connected to the pixel-serial output of the pixel array.

Four inputs are connected to analogue input pins and are intended for monitoring voltages in the neighborhood of the sensor.

The last multiplexer input is connected to the on-chip temperature sensor.

The multiplexer is controlled by an internal register, written through the parallel sensor programming interface.

8.1.7 Programmable Gain Amplifier (PGA)

A voltage amplifier conditions the output signal of the multiplexer for conversion by the ADC. Signal gain and offset can be controlled by a register written through the parallel sensor programming interface.

When connected to the pixel array, the PGA also subtracts pixel black level from pixel signal level when in DS/DR mode.

8.1.8 Parallel Sensor Programming Interface

The sensor is controlled via a number of on-chip settings registers for X and Y addressing, PGA gain and offset, one-off calibration of the column amplifiers, ...

These registers are written by the user through a parallel bus.

8.1.9 12-bit Analog to Digital Convertor (ADC)

The on-chip ADC is a 12 bit pipelined convertor. It has a latency of 6.5 pixel clock cycles, i.e. it samples the input on a rising clock edge, and outputs the converted signal 6 pixel clock periods afterwards on the falling edge.

The ADC contains its own SPI serial interface for the optional upload of calibration settings, enhancing its performance.

The ADC is electrically isolated from the actual sensor core: when unused it can be left non-powered for lower dissipation, and without risk for latch-up.

When used, the input voltage range of the ADC is set with a two-node voltage divider connected to pins VLOW_ADC and VHIGH_ADC.

The ADC has an accuracy of 10 bit at 5 Mhz operation speed.

8.1.10 Temperature Sensor

A PN-junction type temperature sensor is integrated on the chip. The temperature-proportional voltage at its output can be routed to the ADC through one of the six analogue inputs of the multiplexer.

The temperature sensor must be calibrated on a device-to-device base. Its nominal response is -4.64 mV/°C .

8.2 Image Sensor Operation

The following s describe the HAS' two readout mechanisms and give the detailed timing and control diagrams to implement these mechanisms.

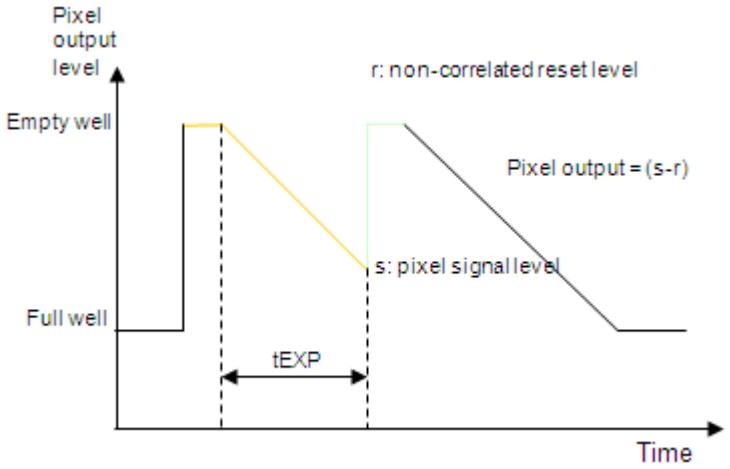
8.2.1 Double Sampling - Destructive Readout

In Double Sampling / Destructive Readout (DS/DR) mode the YRST pointer runs over the frame, top to bottom, each time resetting the line it addresses. Lagging behind this runs the YRD pointer, each time reading out the line it addresses. The distance between the YRD pointer and the YRD pointer is then proportional to the exposure time, hence the electronic shutter operation.

At line readout the signal levels of the pixels in the addressed line are copied onto the column amplifiers' signal sample nodes. Immediately after this the line of pixels is reset, and the pixels' black levels are copied onto the column amplifiers' reset sample nodes. This is destructive readout.

The column amplifiers/PGA then subtract the black levels from the signal levels during sequential pixel out. This is uncorrelated double sampling, eliminating any static pixel-to-pixel offsets of the sensor array.

Figure 31. Double Sampling: Pixel signal is read (s), then pixel is reset, then reset level is read (r)



8.2.2 Correlated Double Sampling - Non-Destructive Readout

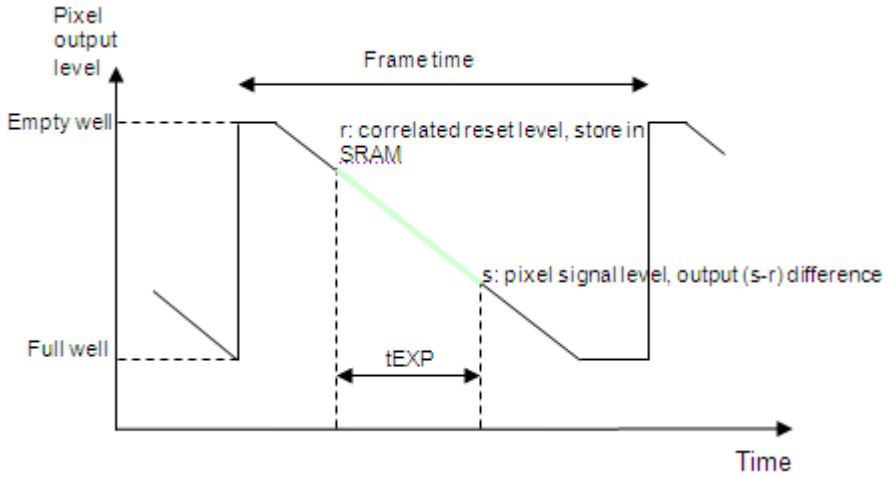
In Correlated Double Sampling/Non-Destructive Readout (CDS/NDR) mode the YRST or YRD pointer quickly runs over the frame, top to bottom, resetting each line it addresses. This leaves the pixel array drained of charges, in black or dark state.

Then the YRD or YRST pointer is run over the region of interest of the frame, and of each line addressed the pixels' black levels are read out and passed on to the ADC. The user stores these black levels in an off-chip frame-sized memory.

Then the system is held idling during the exposure time.

After the exposure time has elapsed, the frame is scanned once more with the YRD or YRST pointer, and each line addressed is read out again. These signal levels are passed on to the ADC and then to the end user. At the same time, the user retrieves the corresponding black levels from the memory and subtracts them from the signal levels. This is correlated double sampling, eliminating static offsets as well as kTC noise

Figure 32. Correlated Double Sampling: Pixel is reset, reset level is read and stored (r), pixel is exposed, signal level is read (s), difference is output



8.2.3 Possible Exposure Times

The range of exposure times attainable by the HAS is entirely dependent on the user control strategy, although two obvious scenarios can be envisaged:

In Destructive Readout/Double Sampling, a typical case would be a minimal exposure time equal to the line readout time, and a maximal exposure time equal to the frame time. With 1024x1024 pixels in a frame, 10 frames per second, this amounts to 98µs and 100ms.

In Non-Destructive Readout/Correlated Double Sampling it is not even possible to pinpoint a typical case, as all depends on the exact reset (R), reset-read (r) and signal-read (s) scheme the user employs. In the specific case of 10MHz pixel rate rate operation, 10 windowed frames per second, and 40 windows of 20x20, each receiving the same exposure time, and the whole FPA reset (R) at the start of the frame, the minimal exposure time would be 7.3ms, the maximal exposure time 90.2ms. Depending on window configuration, shorter and longer times are possible, though.

8.2.4 Timing and Control Sequences

Definitions

The HAS is a line-scan imager with 1024 horizontal lines (Y) each of 1024 pixels (X). Pixel coordinates are defined relative to an origin (X=0,Y=0), and projected onto the user's display view: the origin (0,0) is in the top-left corner of the displayed image, lines are scanned top-down, and the pixels in a line are scanned left to right.

Windows or regions-of-interest are defined by their top-left and bottom-right coordinates (X1,Y1)-(X2,Y2). The full frame then corresponds to (0,0)-(1023,1023). Note that (X1,Y1) is to be programmed into the sensor, while (X2,Y2) is not: windowed readout is obtained by pointing the sensor to (X1,Y1), followed by reading out (Y2-Y1+1) lines of (X2-X1+1) pixels.

A frame readout sequence consists of a number of line readout sequences.

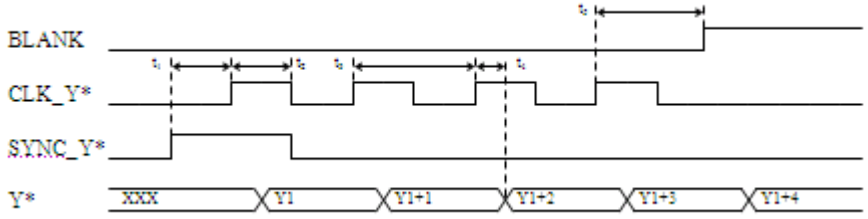
A line readout sequence consists of

- A line select sequence for the YRD and YRST pointer shift registers, during which a line may be selected for readout and another line may be selected for reset
- A line blanking sequence during which the line selected for readout copies its pixel signals into the column amplifiers, the column amplifiers are operated, and both lines selected are optionally reset (the line selected for read can be reset as part of the destructive readout/double sampling operation; the other line can be reset as part of the electronic shutter operation).
- A pixel readout sequence

A pixel readout sequence consists of

- Initialization of the pixel pointer XRD to position X1
- A sequencing through the region-of-interest,
- While the output amplifier and the ADC are activated and pixel values are sequentially selected, connected to the PGA, and converted by the ADC.

Figure 33. Line Selection Timing Diagram



Above timing diagram is valid for CLK_YRD/SYNC_YRD and for CLK_YRST/SYNC_YRST.

	Description	Min	Typ	Max	Remarks
t_1	SYNC_Y* setup	50 ns			
t_2	CLK_Y* high width	100 ns			
t_3	CLK_Y* period	200 ns			No constraint on duty cycle
t_4	Address delay		30 ns		
t_5	Setup to next blanking	100 ns			

Destructive Readout Timing Diagram

n this mode the unit of timing is conveniently chosen to equal the time needed to read out a line of pixels. Hence, the exposure time tEXP can be expressed as an equivalent number of lines.

Table 16. Threads of Operation for Destructive Readout with Double Sampling

Comment	YRD - read side	YRST - reset side
init	Load registers Y1 and X1 with the window start coordinates Initialize YRD with Y1	Initialise YRST with Y1
expose	.do nothing	For YRST = Y1 to Y1+tEXP loop .select line YRST .reset line YRST .wait for one line time .advance YRST one position end loop
read	For YRD = Y1 to Y2 loop .select line YRD .operate column amplifiers for DS/DR .read pixels X1 to X2 .advance YRD end loop	.select line YRST .reset line YRST .advance YRST

Figure 34. DS/DR Sequence: Exposure is initiated with running YRST over the array, resetting lines. After tEXP YRD sTarts running over the array too, reading and then resetting lines

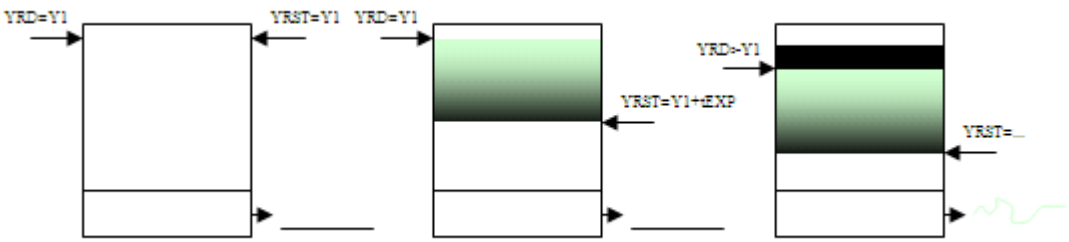
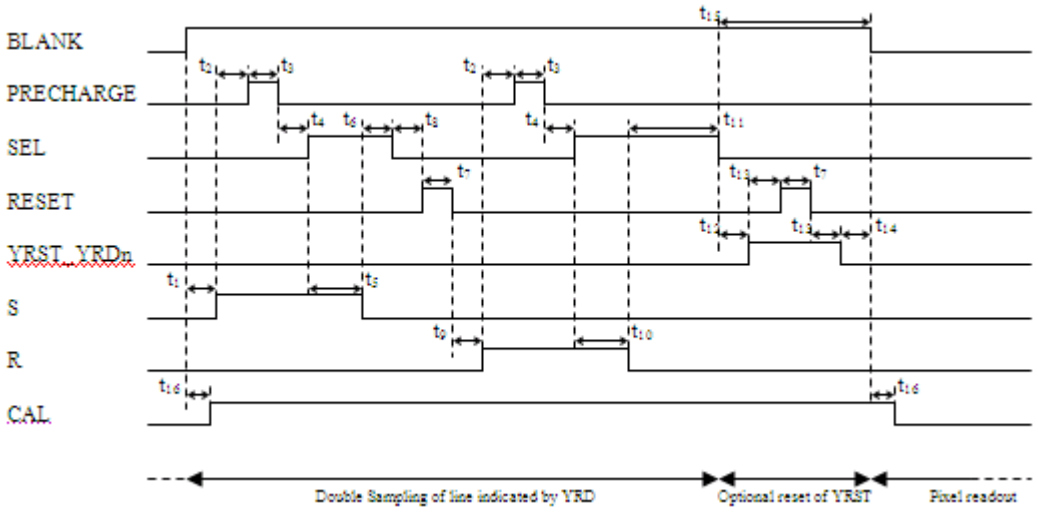


Figure 35. Destructive Readout Timing Diagram



	Description	Min	Typ	Max	Remarks
t_1	BLANK setup	13 ns	25 ns		
t_2	S setup	10 ns	25 ns		
t_3	PRECHARGE width	400 ns			
t_4		30 ns	50 ns		
t_5	S active when SEL	2µs			
t_6		11 ns	25 ns		
t_7	RESET width	400 ns			
t_8		100 ns			
t_9		100 ns			
t_{10}	R active when SEL	2µs			
t_{11}		10 ns	25 ns		
t_{12}	YRST_YRDn setup	100 ns			Second RESET is optional
t_{13}	YRST_YRDn hold	100 ns			
t_{14}	BLANK hold	22 ns	25 ns		
t_{15}	BLANK hold	100 ns			When no second RESET
t_{16}	CAL delay ref. BLANK	25 ns			Once per frame or per line

The CAL signal initiates the programmable gain amplifier to a known 'black' state. This initialization should be done at the start of each frame.

Non-Destructive Readout Timing Diagram

In describing this mode the unit of timing is conveniently chosen to equal the time needed to read out a line of pixels. Hence, the exposure time tEXP can be expressed as an equivalent number of lines. (Note however that the user is under no obligation to link tEXP to the line read time: tEXP can be chosen arbitrarily as its timing and nature are only dependent on the external system controlling the HAS).

Table 17. Threads of Operation for Non-destructive Readout with Off-chip CDS

Comment	YRD - read side	YRST - reset side
init	Load registers Y1 and X1 with the window start coordinates initialize YRD with Y1	 Initialize YRST with Y1
clear frame	.do nothing	for YRST = 1 to 1023 loop .select line YRST .reset line YRST .advance YRST one position end loop
read black levels	for YRD = Y1 to Y2 loop .select line YRD .operate column amplifiers for CDS/NDR, black levels .read pixels X1 to X2 .advance YRD end loop	
exposure	wait for time tEXP	
read signal levels	for YRD = Y1 to Y2 loop .select line YRD .operate column amplifiers for CDS/NDR, signal levels .read pixels X1 to X2 .advance YRD end loop	

Proper operation can be attained by using just one Y pointer register, YRD or YRST, for all of the frame's phases. The above operation scheme is just an example, using YRST for the frame reset phase.

Figure 36. CDS/NDR Sequence: First array is reset completely with YRST. Then black levels are read with YRD. Then, after a time tEXP, all signal levels are read, again with YRD

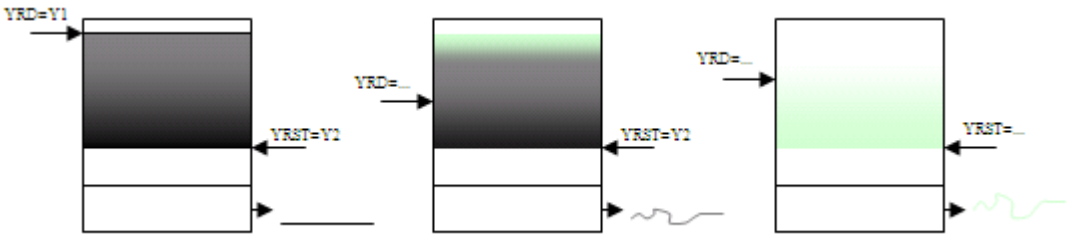
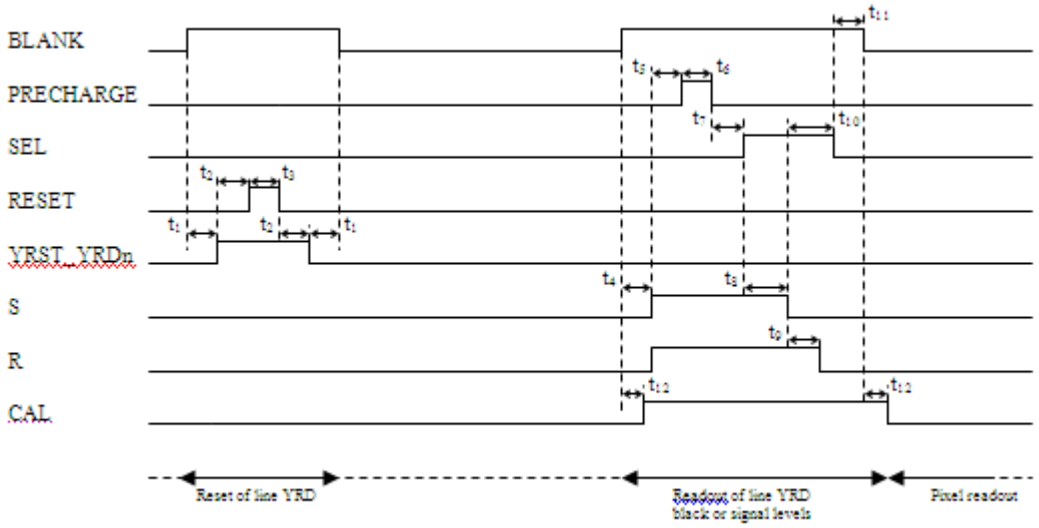
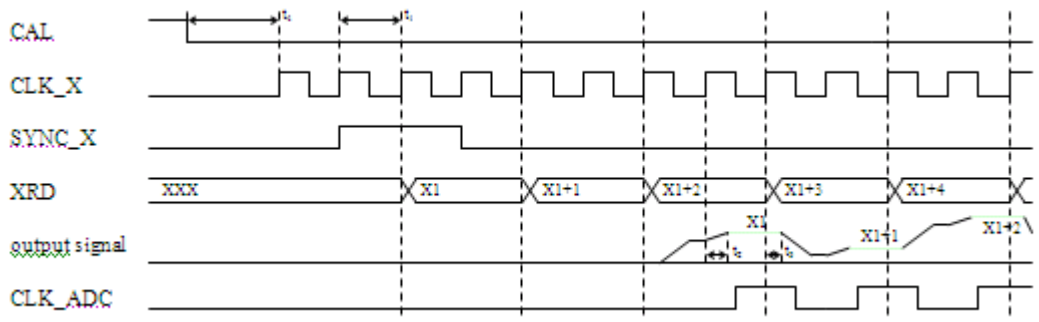


Figure 37. Non-destructive Readout Timing Diagram



	Description	Min	Typ	Max	Remarks
t_1	BLANK setup	13 ns	25 ns		
t_2	YRST_YRDn s/h	100 ns			Optional, only when YRST is used instead of YRD
t_3	RESET width	400 ns			
t_4	BLANK setup	13 ns	25 ns		
t_5	S/R setup	10 ns	25 ns		
t_6	PRECHARGE width	400 ns			
t_7		30 ns	50 ns		
t_8	S/R active when SEL	2.4µs			
t_9		11 ns	25 ns		
t_{10}	SEL hold	11 ns	25 ns		
t_{11}	BLANK hold	100 ns			
t_{12}	CAL delay ref. BLANK	25 ns			once per frame or per line/window

Figure 38. Pixel Readout Timing Diagram



The externally applied clock CLK_X runs at twice the pixel rate. From address pointer XRD shift to output signal available exists a latency of 6 CLK_X cycles. The above timing diagram supposes an ADC sampling at the rising edge of CLK_ADC.

	Description	Min	Typ	Max	Remarks
t_1	CLK_X period	50 ns	100 ns		50% duty cycle required, +/-2.5 ns
t_2	output settle time			15 ns	
t_3	output hold time		2 ns		
t_4	CAL off setup	50 ns			BLANK off setup when no CAL

PGA and Signal Multiplexer Control

Figure 39. Programmable Gain Amplifier and Signal Multiplexer Diagram

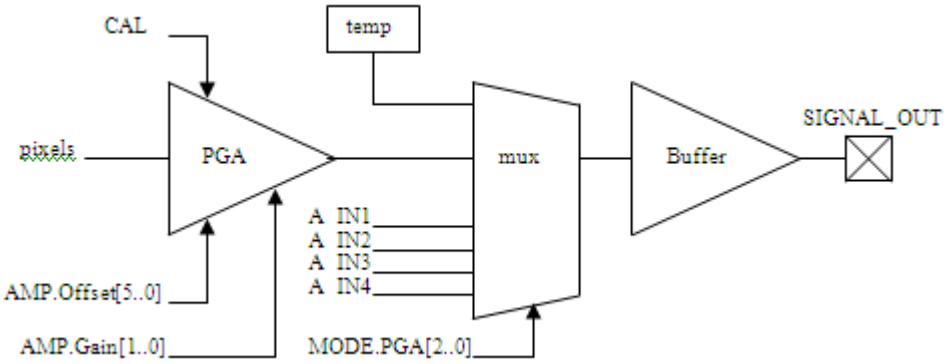
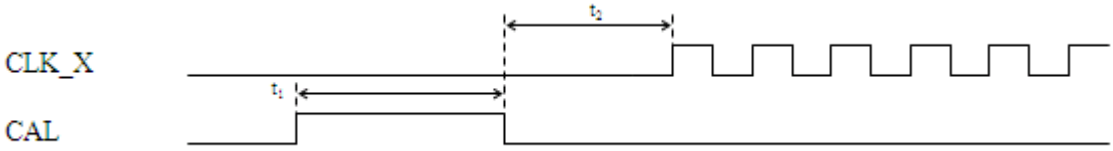


Figure 40. Amplifier Calibration Timing Diagram



The output of the column amplifiers is a stream of raw or FPN-corrected pixels. These pixels then pass the Programmable Gain Amplifier, where gain and DC-offset can be adjusted. Then follows a signal multiplexer that selects between the pixel signal or the temperature sensor and four externally-accessible analogue inputs. The output of the multiplexer is buffered and then made available at output pad SIGNAL_OUT.

The PGA must be calibrated periodically with a black reference input signal, triggered by CAL. After each change of the gain settings, the PGA have to be calibrated to set the correct offset on the PGA. It is suggested to make this CAL signal equal to the BLANK signal.

Remark: The BLANK signal resets the X shift register. So after each active BLANK period, there has to be a SYNCING of the x shift register before reading out any pixel.

For gain and offset control, see section 8.2.5 on page 56.

	Description	Min	Typ	Max	Remarks
t_1	CAL width	200 ns			
t_2	CAL-to-pixel-readout	50 ns			

Multiplexer operation:

MODE.PGA[2..0]	Selected input
000	pixel array
001	TEMP
010	-
011	-
100	AIN1
101	AIN2
110	AIN3
111	AIN4

Changing gain during read out

It's possible to change the gain settings during the read out of 1 line. The following procedure is suggested.

For example: gain changing between pixel 56 and 57

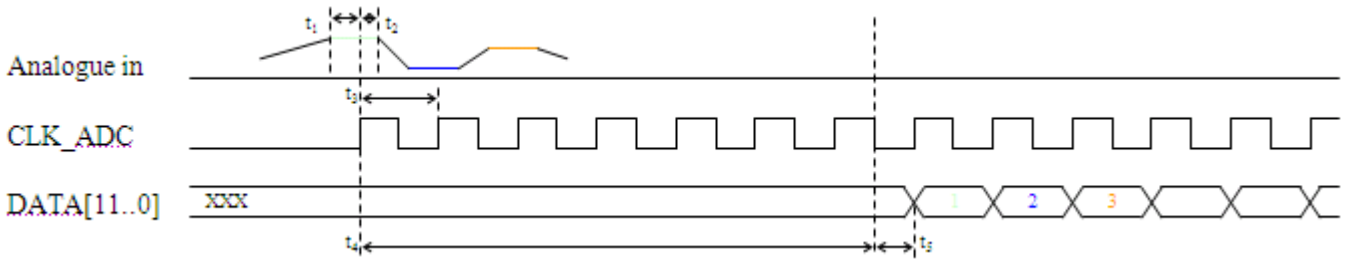
- When pixel 56 comes out, stop the x clock after the falling edge.
- The output stays at the same level of this pixel (see Figure 38 on page 53)
- Change the gain settings by setting the internal registers as described in section 8.2.5 on page 56
- Assert the CAL signal for 200 ns but leave the BLANK signal inactive
- After the CAL signal has felled down, wait 50 ns.
- Reactivate the X clock starting with the rising edge
- The first pixel that comes out is pixel 57

The total time needed to change the gain settings is about 450 ns

Hard Reset - Soft Reset - Hard-to-Soft Reset

See "Reset Modes Timing Controls" on page 61.

Figure 41. ADC Timing Diagram



The ADC is a pipelined device that samples on each rising edge of its clock CLK_ADC. The output DATA is updated on each falling edge of CLK_ADC. There is an input-to-output latency of 6.5 clock cycles.

	Description	Min	Typ	Max	Remarks
t_1	input setup	5 ns			
t_2	input hold	20 ns			
t_3	sample clock	100 ns			50% duty cycle required, +/-5%
t_4	Latency		$6.5t_3$		exact
t_5	output delay		10 ns		

8.2.5 Sensor Programming

Parallel Sensor Programming Interface

The operational modes and start-of-window addresses of the HAS are kept in seven on-chip registers. These internal registers are programmable through a parallel interface similar to the one on the STAR250.

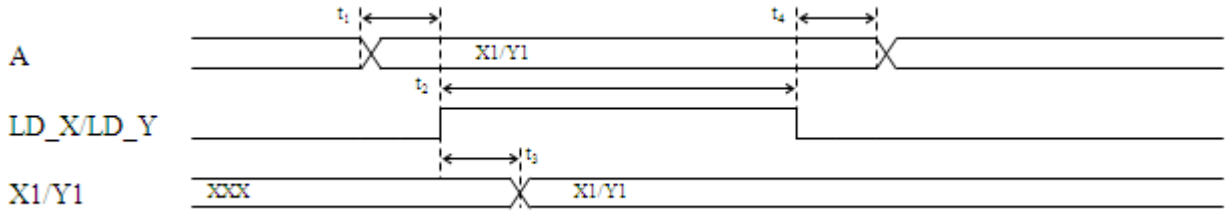
This interface comprises of a 10-bit wide A bus, and 3 load strobes: LD_X, LD_Y, and LD_REG.

With LD_Y or LD_X asserted (rising edge), the full 10 bits of A are loaded into respectively the line start address (Y1) and the column start address (X1) (as similar to the STAR250).

With a rising edge on LD_REG, the upper two bits of A are decoded as an internal register address, and the 8 lower bits of A are loaded into the corresponding register. These 4 registers are reset to their default values by asserting RES_REGn.

Address Register Load Timing Diagram

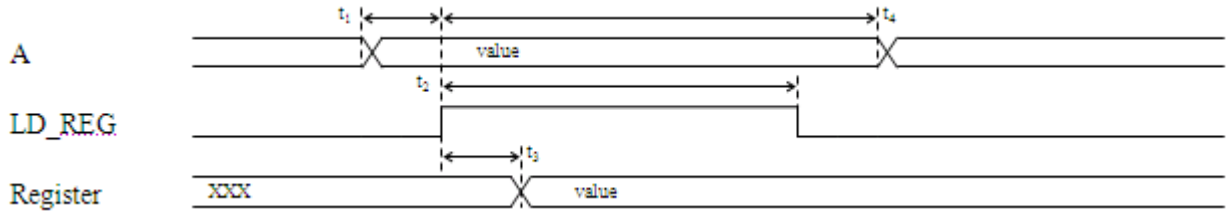
Figure 42. Line/column address upload timing diagram



The YRD/YRST and XRD pointer start address registers Y1 and X1 are latches that pass the input value when LD_Y/LD_X is asserted, and freeze their output values when LD_Y/LD_X is deasserted

	Description	Min	Typ	Max	Remarks
t_1	A setup	100 ns			
t_2	LD_* width	100 ns			
t_3	delay	75 ns			
t_4	A hold	100 ns			

Figure 43. Mode Registers Upload Timing Diagram



The mode setting registers are edge-triggered flip flops that freeze their outputs at the rising edge of LD_REG.

	Description	Min	Typ	Max	Remarks
t_1	A setup	100 ns			
t_2	LD_REG width	100 ns			
t_3	delay	75 ns			
t_4	A hold	100 ns			

Internal Registers Global Description

Are registers are programmed using the parallel upload interface. Two styles of register access methods are used.

Address registers loaded with LD_Y or LD_X:

Register name	Value A[9..0]	Default	Description
Y1	9:0	0	start position of the YRD and YRST one-hot addressing shift registers, range 0..1023
X1	9:0	0	start position of the XRD one-hot pixel address register, range 0..1023

Mode registers loaded with LD_REG and reset to default with RES_REGn:

Register name	Address A[9..8]	Value A[7..0]	Default	Description
MODE	00	6:5	0	End of scan multiplexer
		4:2	0	PGA input multiplexer
		1	0	1 = non destructive readout 0 = destructive readout, dual sampling
		0	0	1 = standby 0 = APS in active mode
AMP	01	7:2	0	Amplifier raw offset
		1:0	0	Amplifier gain.
BLACK	10	7:0	0	NDR mode black level
OFFSET	11	7:0	0	DR mode column bus offset correction

Internal Registers Detailed Description

X1 Register:

X1		strobe: LD_X
A[9..0] = X1[9..0]		
X1[9..0]		start coordinate of XRD shift register for pixel scan

Y1 Register:

Y1		strobe :LD_Y
A[9..0] = Y1[9..0]		
Y1[9..0]		start coordinate of YRD and YRST shift registers for line scan

Legal (decimal) values are 0 (first line of the array) to 1023 (last line of the array)

MODE Register:

MODE	A[9..8] = “00”	LD_REG
A[7..0] = “X”&EOS[2..0]&PGA[2..0]&NDR&StandBy		
EOS[1..0]		End-Of-Scan indicator selector
	00	output of YRD shift pointer register to pin EOS
	01	output of YRST shift pointer register to pin EOS
	10	output of XRD shift pointer register to pin EOS
	11	output of XRD shift pointer register to pin EOS
PGA[2..0]		PGA input multiplexer

MODE	A[9..8] = “00”	LD_REG
	000	pixel array
	001	TEMP temperature sensor
	010	-
	011	-
	100	AIN1 analogue telesense input
	101	AIN2
	110	AIN3
	111	AIN4
NDR		Non-Destructive Readout selector
	0	NDR off, DS/DR enabled
	1	NDR on, CDS/NDR enabled
StandBy		power switch
	0	sensor operational
	1	sensor in standby / low power

EOS[1..0] connects the output of the last stage of either one of the internal array=addressing shift register pointers YRD, YRST or XRD to the outside world at pin EOS.

PGA[2..0] selects one of 6 possible analogue signals to be connected to the analogue output pin.

NDR selects DR or NDR mode.

Standby puts the sensor in a low-power mode, in which the current mirror bias network drivers of the column structures, PGA, output buffer, and internal offset DACs are disabled.

AMP	A[9..8] = “01”	LD_REG
A[7..0] = Offset[5..0]&Gain[1..0]		
Offset[5..0]		PGA offset
Gain[1..0]		PGA gain
	00	1
	01	2
	10	4
	11	8

This register sets the Programmable Gain Amplifier's output offset and gain. The PGA output signal offset is controlled in 64 steps of 16 mV each, from 0.3 V to 1.3 V. Output offset control is used to adapt the PGA's output to the ADC used (internal or external ADC). See “Other definitions:” on page 3.

For unity gain and internal ADC use, the recommended default setting is:

AMP_OFFSET = 60

The reset value of AMP.Offset is 0, decoding to the middle offset value of 0.8V. AMP.Offset range 0 to 31 corresponds to levels of 0.8 to 1.3V, while AMP.Offset range 32 to 63 corresponds to levels of 0.3 to 0.8V.

Gain is controlled in 4 steps for nominal values of 1,2,4, and 8. Real gain values are expected to be somewhat lower and will be characterized.

BLACK Register:

BLACK	A[9..8] = “10”	LD_REG
A[7..0] = BLACK[7..0]		
BLACK[7..0]		NDR mode black level

The BLACK register sets the black level of the column amplifier structures and column prechargers when used in NDR mode.

The reset value of BLACK is 0, setting the internal black level to half-way full scale: BLACK range 0..127 corresponds to 1.65V to 2.9V in steps of 10mV. BLACK range 128 to 255 corresponds to 0.4V to 1.65V in steps of 10 mV.

The recommended default setting is:

BLACK = 10

OFFSET Register:

OFFSET	A[9..8] = “11”	LD_REG
A[7..0] = OFFSET[7..0]		
OFFSET[7..0]		Column bus offset correction.

The column signal path and later parts of the signal path is split in an odd bus with amplifiers and an even bus with amplifiers.

Using the OFFSET register, the offsets for these two signal paths can be calibrated to obtain a balanced performance.

The reset value of OFFSET is 0, driving the offset generator to half-scale (0mV) . OFFSET range 0 to 127 corresponds to 0 to +17.5mV in steps of 140µV. OFFSET range 128 to 255 corresponds to -17.5mV to 0mV in steps of 137µV.

Expressed in electrons, this gives the following numbers:

Total offset correction range: 2365 electrons

Step of correction: 9.3 electrons

The recommended default setting is:

OFFSET = 0 (sample depended).

It's recommended to calibrate the device while taking a dark image.

8.2.6 Sensor Calibration

NDR Mode Black Level

BLACK=10.

Column Amplifier Offset Correction

The column amplifier structures comprise of two independent signal buses, one handling pixels from odd columns, one handling pixels from even columns.

As these structures are inherently imperfectly matched in offset, user calibration of this parameter is required when the sensor is operated in destructive readout / double sampling mode.

The default (reset) values for this parameter puts the internal calibration signal generators in their neutral, middle-value mode.

ADC Corrections

Concept

The ADC is a pipelined device with 11 identical conversion stages in series. Each conversion stage is built around an amplifier with calibratable gain. Each amplifier's gain can be tuned individually with an 8 bit code, totaling 11 words of 8 bits to be loaded into the ADC through a separate serial interface.

ADC Tuning Codes

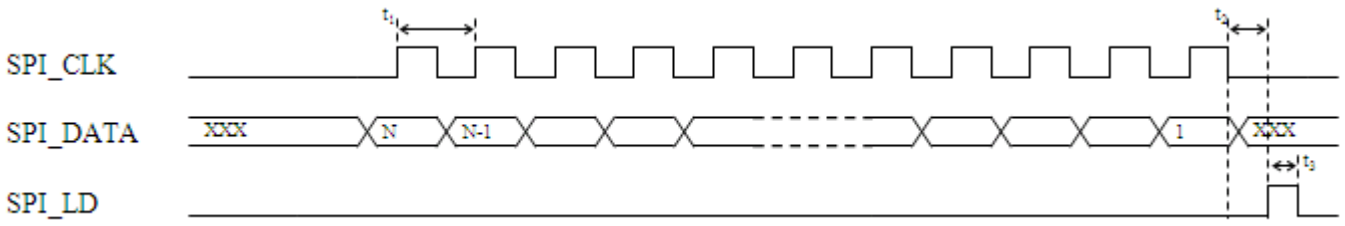
Tuning codes each span the range 0 to 255, with value 127 denoting the amplifier's central gain setting (default after power-on, i.e. without user calibration, and allowing nominal operation of the device). Code 0 reduces the gain with 5%, tuning code 255 increases gain with 5%. The code-gain relation is guaranteed monotonous.

ADC Linearity Tuning Method

The ideal calibration code is 75 for each stage.

It is expected that a complete set of calibration values will be provided in the sensor datasheet, or when necessary, with each device individually.

ADC Serial Interface



	Description	Min	Typ	Max	Remarks
t_1	SPI_CLK width	1000 ns			
t_2	SPI_LD setup	0 ns			
t_3	SPI_LD width	1000 ns			

All 11 8-bit correction words are uploaded in one burst of 88 bits. The word for stage 11 first, then stage 10, and so down to stage 1. Within each word the MSB comes first. Bits are sampled on the rising edge of SPI_CLK, and thus should change on the falling edge of SPI_CLK. The complete set of words is registered in the ADC on the rising edge of SPI_LD.

8.2.7 Sensor Biasing

The operating points of the sensor and ADC's analogue circuitry are set with external passive components (resistors and capacitors). These components have their recommended values listed in "Detailed Information" on page 3 (pin list).

ADC Input Range Setting

The input voltage range of the ADC (pin ADC_IN) is to be matched to the signal at hand, in this case the output voltage range at pin SIGNAL_OUT.

The lower threshold is set to the voltage injected at pin VLOW_ADC. The upper threshold is set to the voltage injected at pin VHIGH_ADC. For both settings it is recommended to use a resistive voltage divider: 90 Ohm from GND_ADC_ANA to VLOW_ADC, 130 Ohm from VLOW_ADC to VHIGH_ADC, 130 Ohm from VHIGH_ADC to VDD_ADC_ANA.

8.2.8 Temperature Sensor

An internal temperature sensor presents a temperature-dependent voltage which can be made available at pin SIGNAL_OUT through the multiplexer.

The voltage-temperature dependency is approximately -4.64 mV/°C, but the absolute level is to be characterized on a device-by-device basis for demanding applications.

With the on-chip ADC biased for an input window of 0.7 to 1.9 V, the temperature sensor/ADC combination can be used from -40 to +125 °C.

8.2.9 Reset Modes Timing Controls

Figure 44. Hard Reset

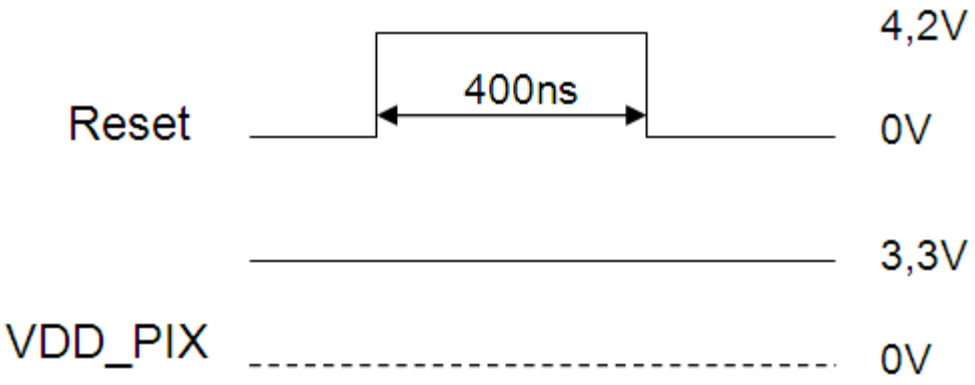


Figure 45. Soft Reset

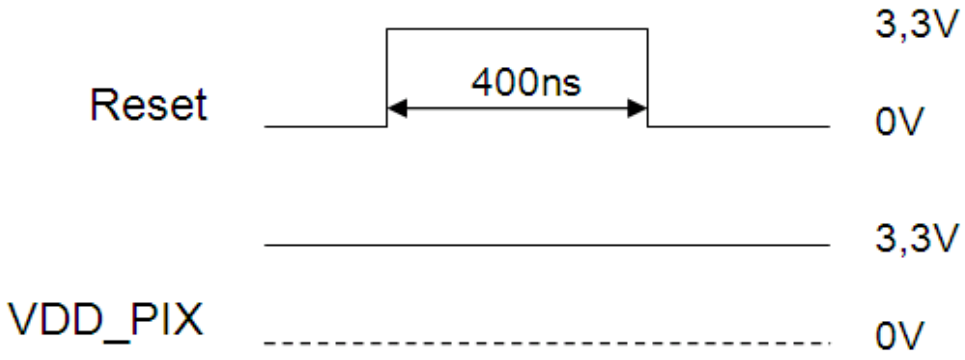
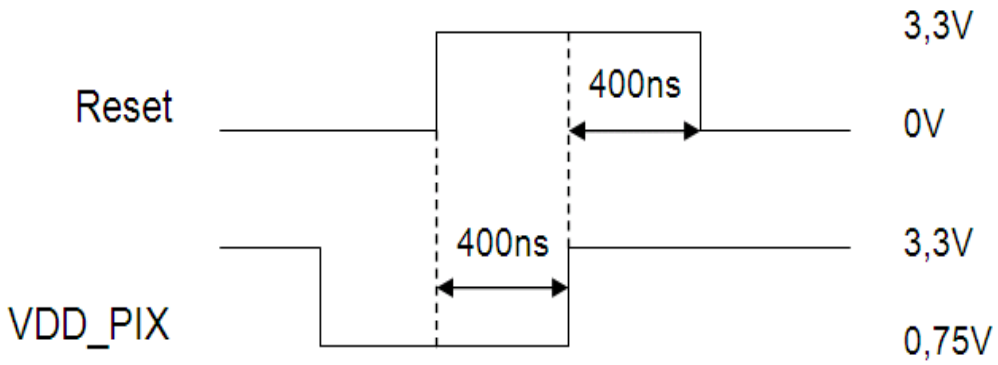
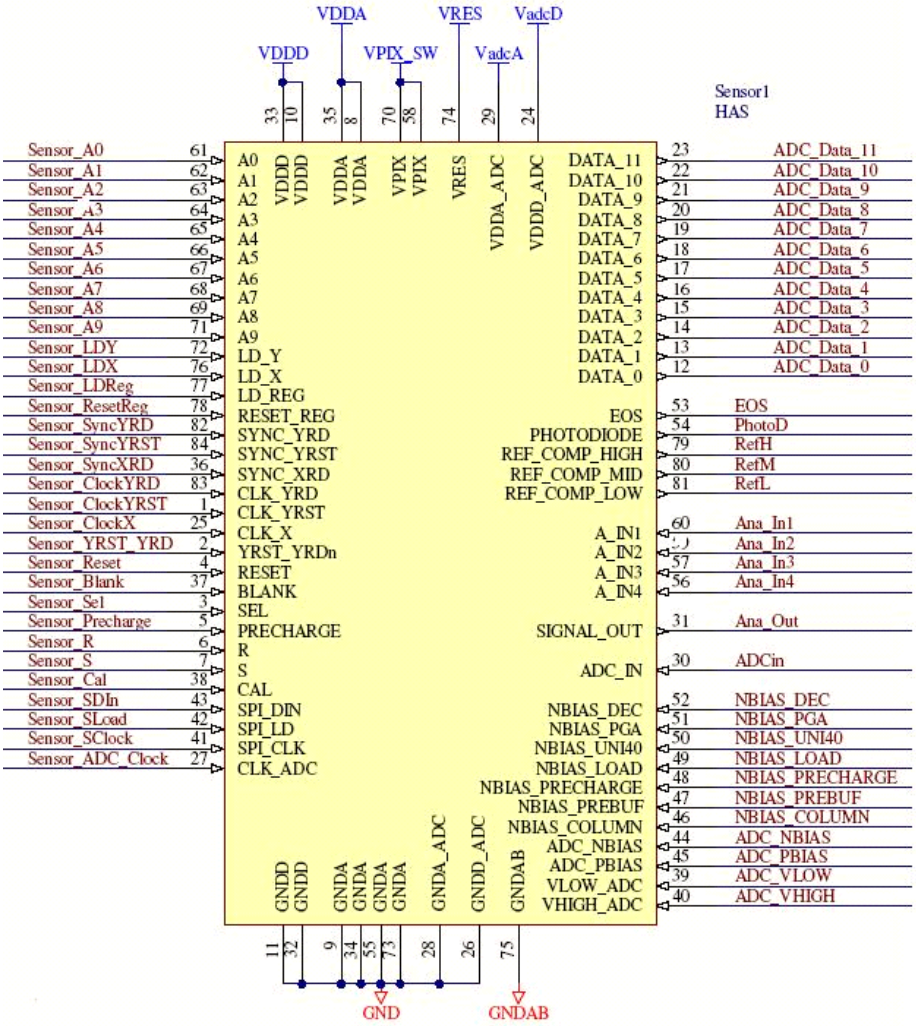


Figure 46. Hard to Soft Reset



8.3 Application and Test Circuits

Figure 47. Sensor Pinning



All ground pins may be connected to 1 point except the anti blooming ground (GNDAB).

Figure 48. Sensor Biasing Circuits

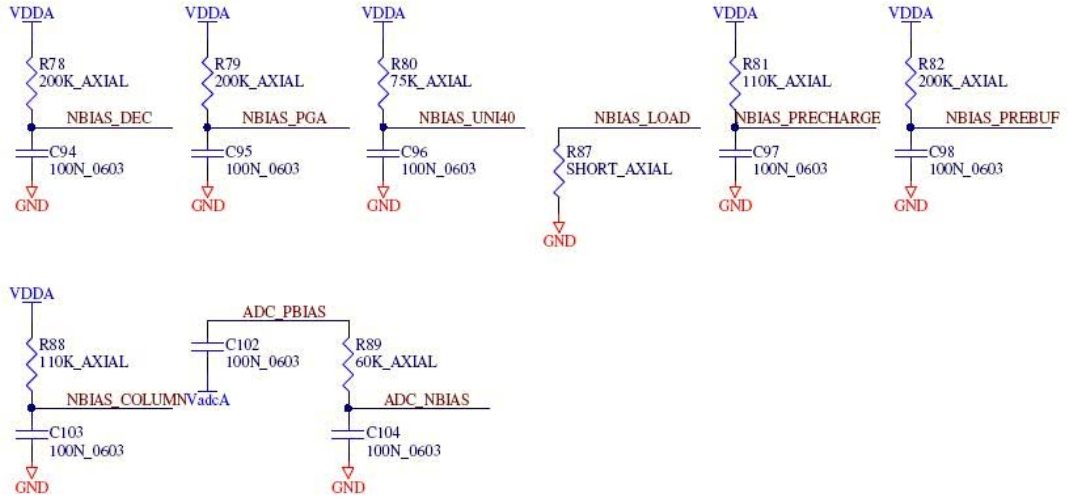


Figure 49. Sensor Power Supply Decoupling Circuits

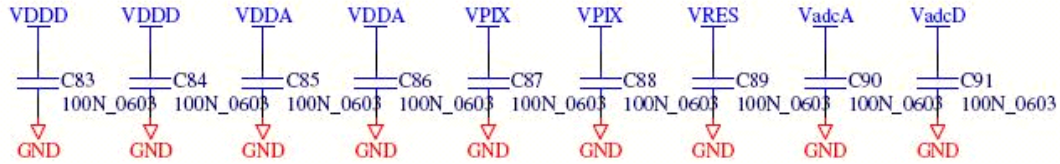


Figure 50. Reference Voltages End Circuit

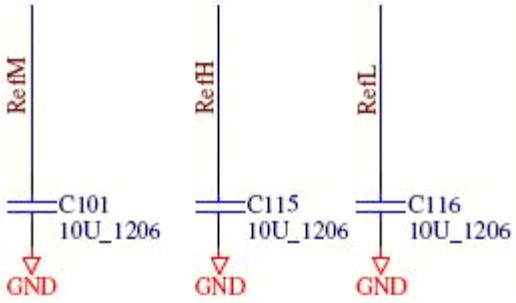
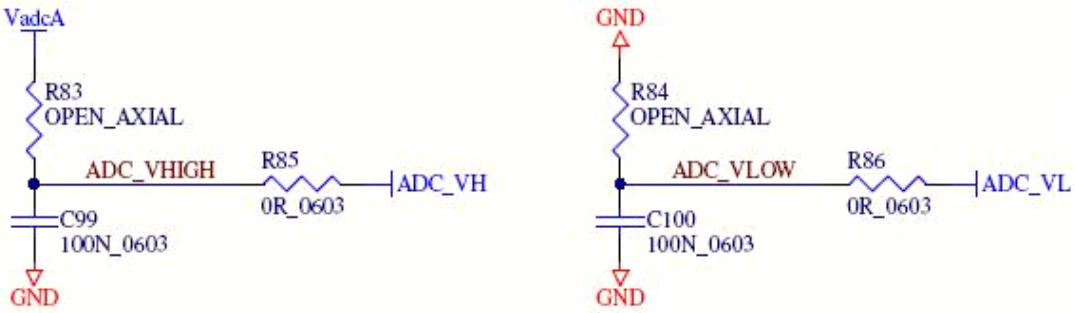


Figure 51. Sencor ADC Circuitry



The reference voltages can be either injected by a power supply voltage or can be generated from a resistance divider. See “ADC Input Range Setting” on page 60.

8.4 Device handling

8.4.1 Handling Precautions

The component is susceptible to damage by electro-static discharge. Therefore, suitable precautions shall be employed for protection during all phases of manufacture, testing, packaging, shipment and any handling.

Until proven otherwise by evaluation testing these devices must be considered as Class 0 in the HBM ESDS component classification. This specification can possibly be widened when the results of the evaluation test program are known.

8.4.2 Storage Information

The components must be stored in a dust-free and temperature-, humidity and ESD controlled environment.

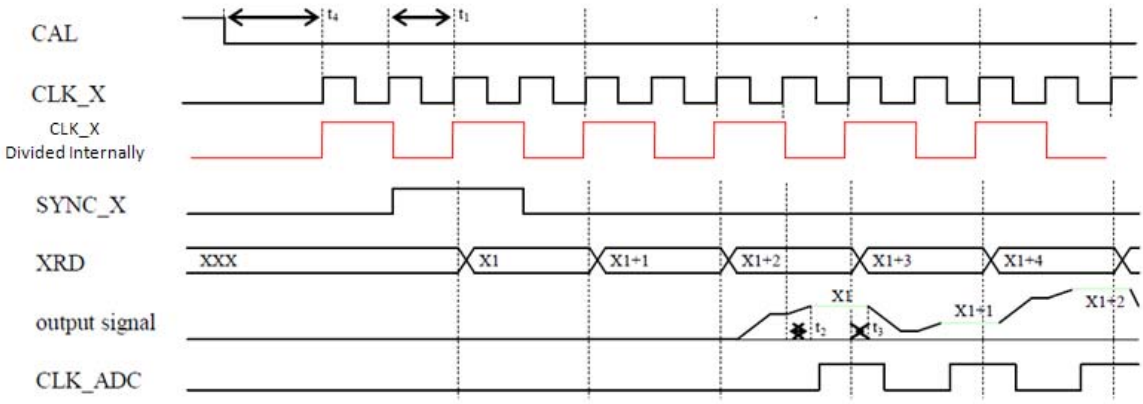
The specific storage conditions are mentioned in Table 2 on page 9 of this specification.

9. Frequent Asked Questions

Question:

In my datasheet for the HAS2, the pixel readout timing diagram is lacking some information I need. It appears SYNC_X should change on the rising edge of CLK_X. And while SYNC_X is high, a rising edge of CLK_X should sync XRD to X1 register. But the diagram shows SYNC_X high for 2 CLK_X periods. Due to timing variations, SYNC_X could technically be high for as many as 3 different rising edges of CLK_X! The timing diagram doesn't show any setup or hold timing for SYNC_X and CLK_X.

Answer:



CLK_X is divided internally in the sensor. SYNC_X is based upon this divided clock. When SYNC_X is high for a even pair of this divided clock cycles the XRD will be pushed the length of this even pair of clock cycles. Though, when SYNC_X drops during an un-even pair of divided clock cycles it is unclear what XRD will do. But this behavior is most unlikely.

Question:

RES_REGn doesn't have any timing info either. It's the asynchronous reset for internal registers. How long must it be held low?

Answer:

To be on the safe side you have to keep it low for at least 1us.

You can apply the following sequence when powering up the sensor:

- Power on device with known register settings
- During power on, keep RES_REGn low for at least 1us
- Apply Line/column address upload timing diagram

Question:

The ADC serial interface timing diagram is incomplete. It appears the SPI_DATA is supposed to change on the falling edge of SPI_CLK. If so, then what is the setup and hold times of the SPI_DATA around the rising edge of SPI_CLK? The SPI_CLK has a period of 1000 ns, so the SPI_DATA would be present for 500 ns prior to the rising edge of SPI_CLK. But what is the SPI_DATA setup time for the *first* rising edge of SPI_CLK (first bit of data)?

Answer:

The best way to operate the device is to change your SPI data during the falling edge of the SPI clock. This gives you plenty of time before the data is being sampled on the rising edge of the SPI clock.

But to answer onto the question. You have to consider a 100ns hold and setup time of the SPI data around the rising edge of the SPI clock. Theoretically you are right about the 500ns but please consider 100ns for your timing.

For the first rising edge please consider a 500ns setup time for the SPI data.

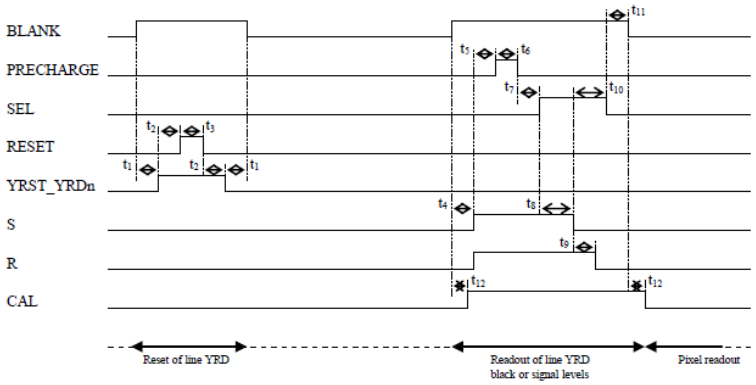
Question:

I noticed that BLANK remains high for the Destructive readout timing diagram, and even during the reset of YRST row. But in the Nondestructive readout timing diagram, you have BLANK shown going low between a reset and line selection, but no timing information regarding that.

What does the timing need to be? Or can I leave BLANK constantly high during a line reset and subsequent line selection during Nondestructive readout?

Answer:

For the non destructive read out you can extend T1 and reduce T4. So meaning that you can leave the BLANK signal high.



Question:

What is your recommendation to do with the unused Analog inputs to the multiplexor (A_IN1-4)? Grounding them would place them at 0 volts which is outside of the VLOW_ADC range. Should they be left floating? Or should they be tied to some constant voltage source between VHIGH_ADC and VLOW_ADC?

Answer:

If you don't use the analog inputs I propose to ground them. But most of our customers are using these inputs to monitor some supply voltages. For example, you could monitor your 3.3V input voltage. Of course you have to divide it with a resistance divider to have the voltage inside the ADC range. You could use it also to monitor some external voltages that are used on your board and which are important to be stable. Just some idea's…

Question:

What are the implications of turning off the analog power supplies (VDDA), but keeping the digital power supply (VDD) active? Is this bad? I'm trying to improve the standby low power mode.

Answer:

No this is not bad. In fact the total power supply current will reduce even a little bit more.

Question:

Spec sheet describes the ADC input range setting: 90 Ohm from GND_ADC_ANA to VLOW_ADC, 130 Ohm from VLOW_ADC to VHIGH_ADC, 130 Ohm from VHIGH_ADC to VDD_ADC_ANA. The VDD_ADC_ANA is 3.3V so this puts VLOW_ADC = 0.85 V and VHIGH_ADC = 2.07 V.

But Table 14 on page 24 lists typical power supply settings and sensor settings: It says ADC_VLOW = 0.8V and ADC_VHIGH = 2.5V.

Which way do you recommend? Can you describe the discrepancy?

Answer:

The correct ADC range is as you described with the resistance divider. An alternative without resistance divider is to directly inject this voltage by a power supply circuitry. This how we do it inside our characterization system.

In that way you can tune your ADC settings as you want.

But if you want to stick with the resistances please use the values as described above.

Table 14 on page 24 is a typo. It should be 0.85V and 2.0V

Question:

In your datasheet, ADC High/Low bias voltages are recommended to be set with a resistive divider. But the datasheet doesn't mention anything about temperature stability. For the STAR-1000, there was an internal resistor between ADC_HIGH and ADC_LOW that had temperature dependence. Because of this, for STAR-1000 designs, I used to set my ADC bias voltages with buffers that would keep the bias levels constant over temperature. Do I need to repeat the same principle for the HAS2? Or does the HAS2 remove any temperature dependence for the ADC bias voltages?

Answer:

For good temperature stability, it is better the same principle as the STAR-1000. So use external buffers to keep ADC_HIGH and ADC_LOW to a fixed voltage level

Question:

In your datasheet, in the "ADC Timing Diagram" on page 55, the table lists t5, output delay, as typically 10 ns. The STAR-1000 had a troublesome output delay variability of 20 - 60 ns, some parts had even 70 ns! Have the digital output drivers been significantly improved for the HAS2 ADC? What are typical rise/fall times for the outputs?

Answer:

The output delay and stability has been improved compared to STAR-1000

Question:

Could you please discuss the differences between BLANK, CAL, and PRECHARGE? The STAR-1000 only had a CAL signal.

Answer:

The extra BLANK signal is used to reset the internal CLKX divider. PRECHARGE is used to pre-charge the column lines and column caps to ground

Question:

I liked the flexibility of the STAR-1000. The HAS2 seems more restrictive. For example, your application note says, "…repeated use of pixel re-addressing (register X1) potentially injects offset-noise into any windows that overlap in Y-coordinates." If I understand correctly, this means I cannot address each pixel along a line individually? I cannot readout every other pixel, or every 2nd, or 5th, or 10th? I have to readout all the pixels in a line? Can you think of any options?

Answer:

You still can start reading at any X or Y position. You have only keep in mind that there is an analog pipeline on the pixel data. So if you individual read 2 pixels of the same line closer together then the analog pipe, the second pixel will be addressed when you are only interested in the first pixel. So when you want to read that second pixel by a new SyncX, it will be the second time you address it.

As a result, there is a risk of a deviated value. Probably some deviated offset on the pixel value. You have probably the same problem with STAR-1000 but maybe the analog pipe is there smaller.

Question:

For NDR/CDS mode, there is parasitic exposure given your suggested algorithm. Can I do this algorithm instead?

a. Reset Row X
   i. Start integration timer
b. Readout Row X
c. Reset Row X+1
d. Readout Row X+1
e. Reset Row X+2
f. Readout Row X+2
g. (repeat to region of interest)
h. (wait for integration timer completion)
i. Readout Row X
j. (wait for time to reset a row)
k. Readout Row X+1
l. (wait for time to reset a row)
m. Readout Row X+2
n. (wait for time to reset a row)
o. (repeat to region of interest)

Answer:

I don't see a problem with your algorithm

Question:

I would be interested to get more insight about the HAS anti-blooming capability. In our target application, we must be able to operate with the sun in our field of view. From initial calculations, this means that we can have a sun spot on the sensor around 50 pxls in diameter, over-exposed by a factor of ~1000 against our other target spots.My questions are :

- What is the role of the anti-blooming ground pin (GND_AB) and how does it impact the sensor behavior?
- Is the anti-blooming capability sufficient to prevent any additional "recovery" time of the sensor?
- What pixel to pixel crosstalk behavior can we expect around the sun spot? 9.8% of the full well (Table 13 on page 24), or ...

Answer:

When a pixel is saturated and even goes to negative voltage levels, it isn't anymore suitable for lower electro potential level to attract new photon-electrons. So the extra photo-electrons can now more easily go to nearby pixels instead of to the pixel where the electrons are generated. This is visible in the image as blooming.

The anti-blooming method is keeping the photo-diode at an attractive electro-potential that still attract new electrons. This can be done by holding the gate of the reset transistor higher then ground level.

The 'row_select' line thats selects a specific row of the pixel array is a digital signal that swaps between 'GND_DIG' and 'VDD_DIG'.

The 'row_reset' line that resets a specific row of pixels uses the same drivers as the 'row_select' line but the lower voltage level isn't 'GND_DIG' but 'GND_AB'.

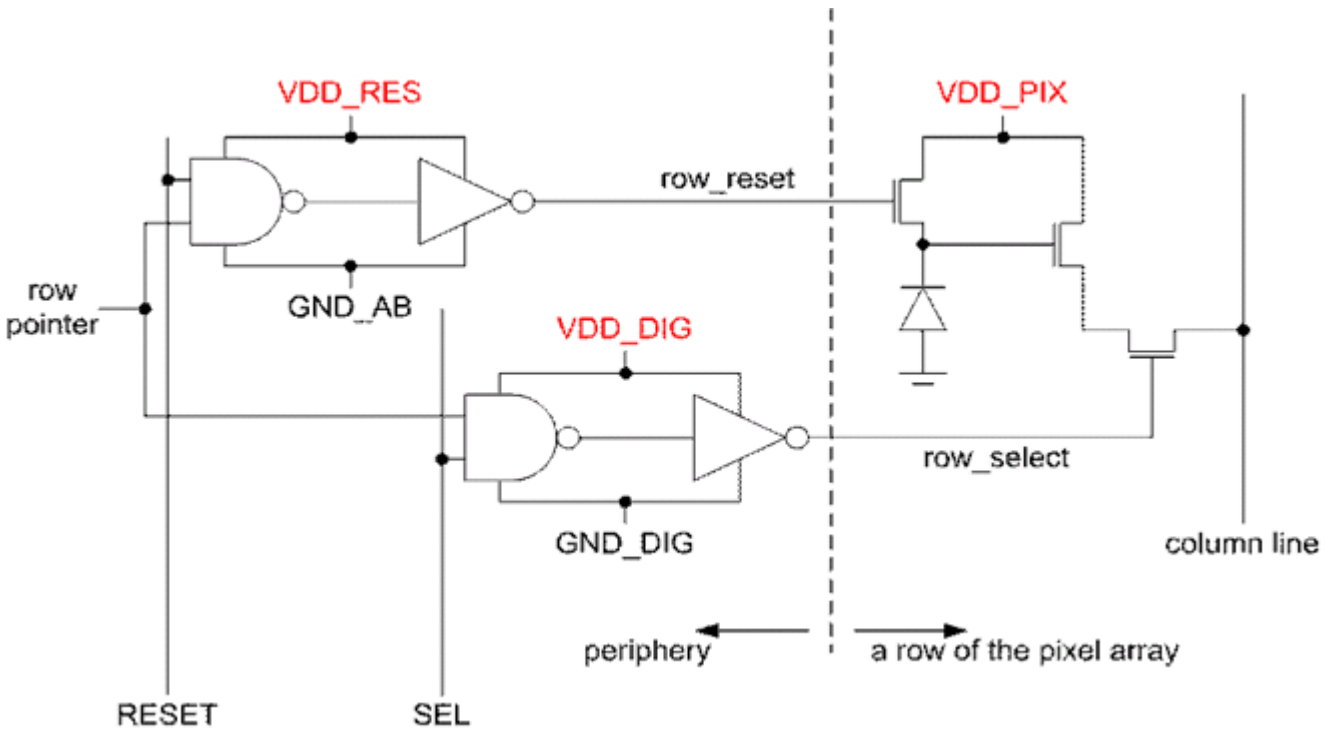
So the lower level of gate of the pixel reset transistor can be set by adapting the voltage level of 'GND_AB'.

It is suggested to not go higher with the voltage level of 'GND_AB' than 1V. The digital circuits of the sensor should still see it as a digital '0'.

Some second order effect of keeping GND_AB higher then ground:

- The swing of row_reset is now lower. This means less cross-talk to the photo-diode and higher dark-level. Probably you don't see much changes if you read the sensor in dual sampling. Both the signal and the dark reference changes in level, so the subtraction is still the same. But you use the photo-diode on a slightly higher voltage level. Therefore, the pixel cap can be a little lower. (Non linear behavior of the cap of a diode).
- The swing of the diode is also lowered, but probably only the part of the swing that was not read-out anyway.

It is very difficult to get any quantification of the anti-blooming effect. The best way of figuring is just trying it. The anti-blooming function is not part of the characterization of the sensor.



Question:

I am trying to estimate the pulse height distribution (PHD) from electrons and protons traversing the focal plane array. The PHD is the probability of seeing a pulse of a given size in a single pixel from an

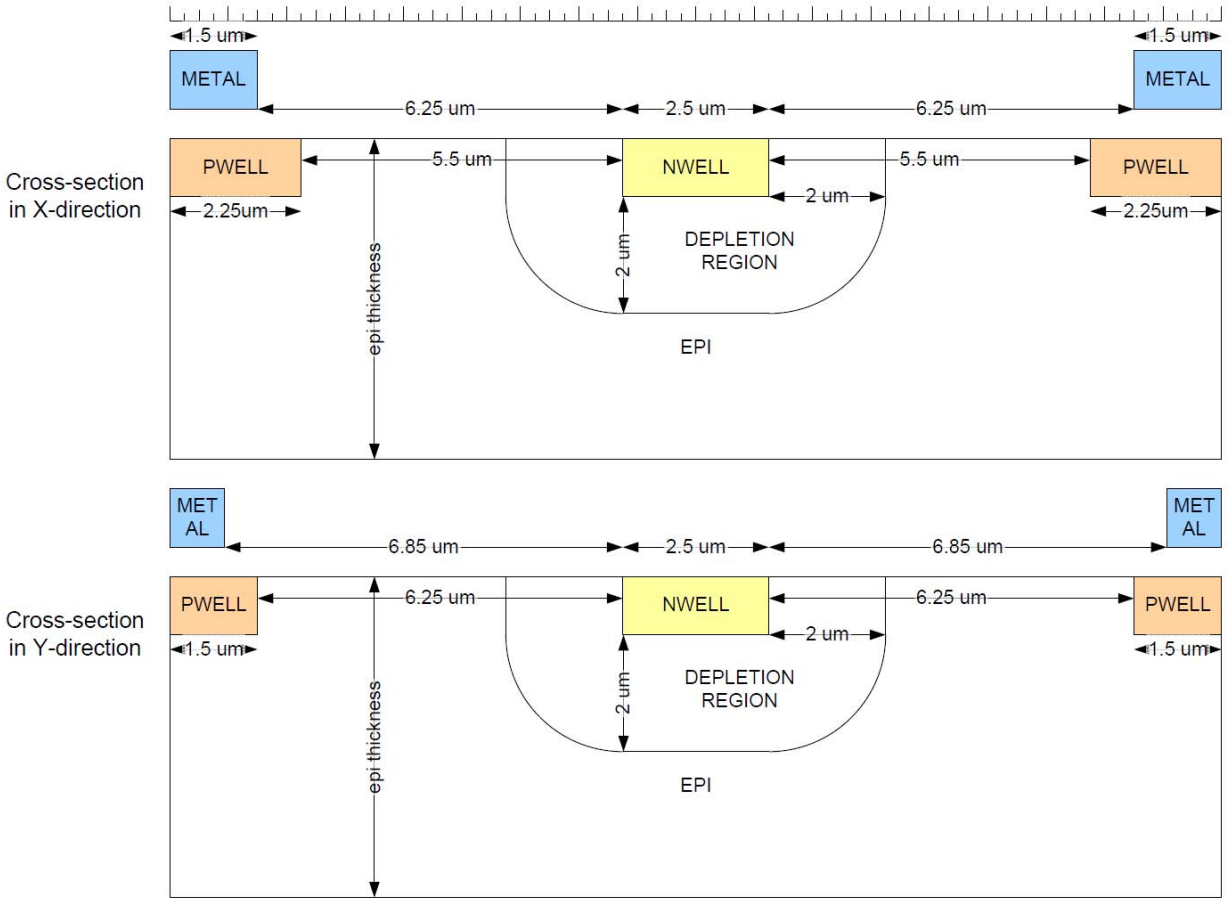
electron or proton coming from a random direction and striking in a random location. When an electron traverses a unit cell it excites electrons. The total amount of charge is proportional to the length of

the path (the chord length) through the unit cell. Charge that is created outside the collection region of the detector has little effect. The charge in the photodiode is collected and looks like signal. In order to calculate the chord length distribution through the photo-diode I need its dimensions. I have been assuming that it is 7.5 microns on a side, living within the 15 micron unit cell. The thing I have no clue

about is the thickness of the collection region. It could be quite thick, but I have been assuming a fairly thin geometry. The production of streaks by protons is sensitive to the thickness of the photodiode as well (thicker means longer streaks). >So I think the answer to your question is that I need all three

dimensions of the photodiodes in the array. I would also like to know if the unit cells are simply repeated across the array or if they are arranged with mirror images next to each other (or something like that) which would make the light sensitive regions cluster in groups of two or four.

Answer:



Question:

Will pixel-to-pixel crosstalk only appear if a pixel is fully saturated? Or will it also appear if for instance the pixel is only as half it's full well capacity. If it does happen even if the pixel is not fully saturated do you know to what extent it will happen - will it also be the same extent as shown in "Pixel-to-Pixel Cross Talk" on page 38 of your datasheet? Will pixel-to-pixel crosstalk only lead to charge leaking from a pixel with higher signal to a pixel with low signal or vice versa?

Answer:

The pixel-to-pixel crosstalk chown in "Pixel-to-Pixel Cross Talk" on page 38. is cross-talk caused by floating generated electrons that are not yet captured by any photo-diode. So it has nothing to do with the actual level on the accumulated photo-diodes. Only when the photo-diode is really totally saturated, the floating electrons can behave differently. The saturated photo-diode cannot capture more electrons, so incoming electrons are not kept. The generated electrons will be captured by neighboring photo-diodes that are not yet completely saturated (or recombined).

So cross-talk as measured in "Pixel-to-Pixel Cross Talk" on page 38 goes both from pixel with higher to lower signal levels and vice versa. It doesn't matter as long they are not fully saturated. Note that the anti-blooming ground can keep the pixel out of a completely saturation state.

Question:

The test results after proton beam are not as expected. In order to interpret the results we want to know what the thickness is of the epitaxial layer. Ore more in detail the thickness of the active area of the photo diode.

Answer:

EPI thickness: 5µm, the nwell is about 1um deep.

Question:

How large is the active area compared to the overall pixel?

Almost the whole photo-sensitive area is active area.

Answer:

96% of the whole pixel is active area. Everything expect the transistors and nwell, is p-doped

Question:

Is there a spice model available for the radiation hard pixel used in the HAS device?

Answer:

No. The models that are used are just non-radiation hard models.

Question:

What is the penetration depth of photons in the HAS2 pixel versus the spectral range? Doe we have such graphs available?

Answer:

This is theory. We have penetration versus spectral range but this depends on the actual doping levels of the substrate. So it is never actual measured.

Question:

How would the MTF behave with increasing wavelength? Is there an MTF graph available versus spectral range?

Answer:

You can expect a large decrease in MTF when using higher wavelengths. To known how it behaves on the HAS2, new MTF measurements are needed.

Question:

In chapter 6.2 of the actual data sheet it is suggested to use one regulator for all digital supply pins together, one regulator for the sensor core analogue supplies together, and one regulator for the ADC analogue supply. Against it the test circuit in chapter 7.3 uses 5 different supply voltages (VDDD, VDDA, VPIX, VadcA, VadcD).

With the first information I decided to use 3 regulators: One for VDD_ANA + VDD_PIX, one for VDD_DIG + VDD_ADC_DIG and one only for VDD_ADC_ANA. Moreover I use two grounds (analog and digital). Sadly with this configuration I have some problems in Window-Mode. Every 2nd line of the first lines of a window overshoot there. The more lines are sampled the lower is that effect. After may be 20 to 30 lines the effect exists no longer. In an other PCB I use a separate regulator for VDD_PIX instead for VDD_ADC_ANA (VDD_ADC_ANA is connected to VDD_ANA) and everything works fine. Could that may be the problem or do you have any other ideas?

Answer:

I expect that the peak currents of VPIX make the power regulator that you use unstable. This is no problem as long the VPIX isn't use by other parts of the sensor.

So it is normal that when VPIX has its own regulator, nothing strange becomes visible in the image. But probably, VPIX is still not stable. However, the double sampling (both the signal and the black level are affected by the voltage level of VPIX) hide the problem for you.

10. Addenda

AN-APS-FF-WO-06-001 (v1.): Application note on HAS readout methods

11. Optical quality - Definitions

The following definitions and limits are used to define the optical quality of the HAS2 type variants as outlined in Table 1 on page 8 of Section "Specification Tables" on page 8.

Dead Pixel

A dead pixel is defined as a pixel which has no electrical response. In the image this is resulted in a pixel with fixed ADC value. The number of pixels with ADC value 0 are count and accumulated.

Bright Pixel in FPN image

A FPN image is defined as a dark image with the shortest possible integration time. A bright pixel in this image is defined as a pixel with an ADC value higher then 20% of the full range of the entire pixel array.

Bad Pixel in PRNU image

A PRNU image is defined as an image where all pixels have a 50% response of the full range of the entire pixel array. A bad pixel in this image is defined as a pixel with an ADC value that differs more then 10% of the average response. This average reponse can be calculated on the total pixel array for a global measurement or on 32x32 pixels for a local measurement.

Bad Row/Column

A bad row/column is detected in the PRNU image. A row / column is defective when it differs more then 5% from the average of a moving window of 32 rows/columns. A row/column is also defined as defective when it has 100 or more adjacent bad, bright or dead pixels.

Document History Page

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**	2725727	FVD	See ECN	Initial Release
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